PL-2

CTV

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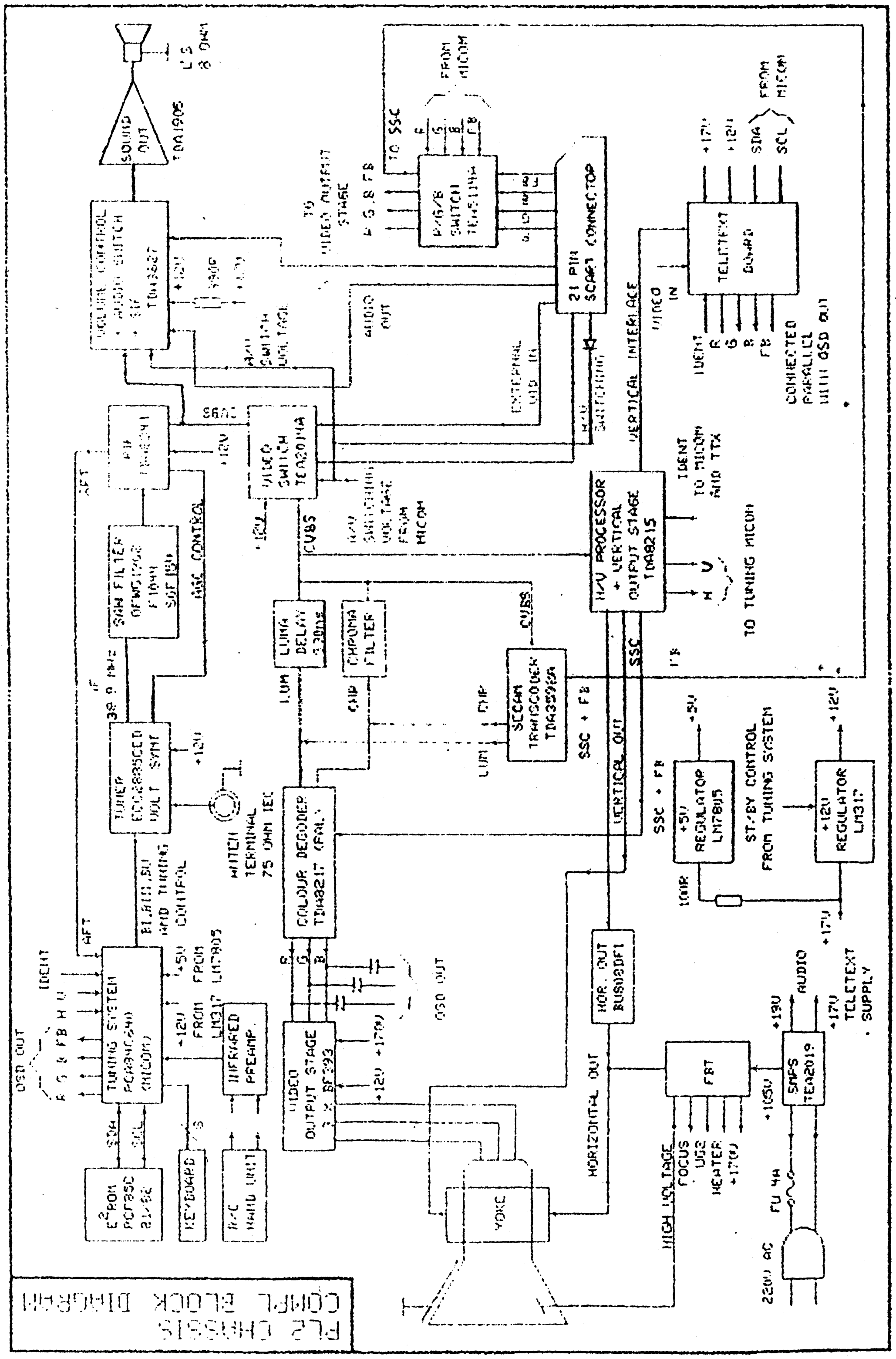
ELECTRICAL ALIGNMENT

POWER SUPPLY


FL2 CHASSIS
COMPL BLOCK DIAGRAM
L'S 8 OHM
SOUND OUT TDA1905
VOLUME CONTROL + AUDIO SWITCH + SIF TDA3827
5.5MHz
AUDIO SWITCH VOLTAGE
AUDIO OUT
TO VIDEO OUTPUT STAGE R G B FB
R/G/B SWITCH TDA3114A
FROM MICOM
TO SSC
21 PIN SCART CONNECTOR
EXTERNAL VID IN
SWITCHING
VERTICAL INTERLACE
VIDEO IN
TELETEXT BOARD
+17V +12V SDA SCL FROM MICOM
IDENT R G B FB
CONNECTED PARALLEL WITH OSD OUT
PIF TDA4501
VIDEO SWITCH TEA2014A
+12V
SWITCHING VOLTAGE FROM MICOM
CVBS
H/V PROCESSOR + VERTICAL OUTPUT STAGE TDA8215
IDENT TO MICOM AND TTX
H V TO TUNING MICOM
SAW FILTER
AGC CONTROL
AFT
LUMA DELAY
CHROMA FILTER
SECAM TRANSCODER TDA3592A
LUM CHR
SSC + FB
SSC
FB
VERTICAL OUT
38.9 MHz IF
TUNER
ANTEN TERMINAL 75 OHM IEC
COLOUR DECODER TDA8217 (PAL)
+5V REGULATOR LM7805
ST-BY CONTROL FROM TUNING SYSTEM
+12V REGULATOR LM317
+5V +12V +17V
100R
IDENT
AFT
BL, BH, BU AND TUNING CONTROL
+5V FROM LM7805
+12V FROM LM317
R G B
OSD OUT
TUNING SYSTEM PCA84C640 (MICOM)
R G B FB H V
INFRARED PREAMP.
VIDEO OUTPUT STAGE 3 X BF393
+12V +170V
HOR. OUT BU508DF1
HORIZONTAL OUT
FBT
SMPS TEA2019
+13V AUDIO
+17V TELETEXT SUPPLY
+105V
HIGH VOLTAGE FOCUS UG2 HEATER +170V
FU 4A
220V AC
SDA SCL
E²ROM PCF85C 81/82
KEYBOARD
R/C HAND UNIT
YOKE

HIGH VOLTAGE TEST :

There is no high voltage adjustment component on the chassis. Changing of + 107V depends on the supply voltage. If it's necessary to measure high voltage;

1- Connect the + probe of high voltage tester to the anode of CPT.

2- Adjust contrast and brightness to minimum.

3- Measure the high voltage as 23.5KV. that voltage is 24.5KV for 20" (51cm) screen size.

4- For maximum brightness, high voltage must be 22.5KV for 51cm.

ADJUSTMENT OF HORIZONTAL OSCILLATOR :

For the adjustment of horizontal oscillator C601 capacitor must be SHORT-CIRCUIT. Adjust P601 , until obtain an optimum stationary picture.

ADJUSTMENT OF HORIZONTAL POSITION :

1- Apply the circular + cross-hatch test pattern to RF input.

2- Center the circle by using P601.

ADJUSTMENT OF SUPPLY VOLTAGE :

1- Make the volume , brihtness and contrast adjustment to minimum.

2- Adjust the supply voltage on the pin of C118 capacitor as 107V by using P100.

FOCUS ADJUSTMENT :

Adjust the thickness of lines until being minimum, by focus trimpot on the EHT transformer. By using cross-hatch or multi-burst test pattern.

38.9 MHZ PIF ADJUSTMENT :

1- Disconnect the if output of tuner from if input.

2- Apply 38.9mhz white-picture to if input.

3- Connect the oscilloscope to video output.

4- Adjust the video signal by using L206 coil shown in the figure 1.

5- Make AFT adjustment after 38.9mhz adjustment.

AGC DELAY ADJUSTMENT :

1- Apply pal colour bar signal which is 60dB uV amplitude (1mV) to the RF input.

2- Turn P200 which is AGC delay control trimpot to the clock-wise u to the end.

3- Adjust P200 until find a picture without snowy.

AFT ADJUSTMENT :

1- Disconnect the if output of tuner from if input.

2- Aply 38.9mhz signal with a pm5518 philips pattern generator to if input.

3- Connect a digital voltmeter to AFT pin of if.

4- Adjust L207 coil until the voltage of AFT pin of if is being 6V DC.

5- Connect the if input which is disconnected in the beginning.

COLOR SYNC ADJUSTMENT :

1- Apply colour bar signal to RF input.

2- Connect a 8K2 resistor between the pins 8 and 16 of IC500 also connect pin 12 to ground. (Make contrast, brightness and colour adjustment to min).

3- Adjust the color syncronisation by using CT500 trimmer cap to the best position.

4- Remove 8K2 resistor and ground connection.

COLOUR GAIN AND PHASE ADJUSTMENT :

1- Apply pal demodulator signal to RF input.

2- Connect the oscilloscope to the blue signal output.

3- Adjust the hanover bars to G-Y=0 level by using L501 coil then make min -V , +V changing of the hanover bars by using P500. Likewise, test the other alternatives.
Signal : color bar pattern , Adjustment : P500 min. hanover bars.

SECAM CHROMA ADJUSTMENT :

1- Apply secam color bar signal to RF input.

2- Connect the channel 1 of oscilloscope to pin 3 of IC 700 and the channel 2 to pin 20 of IC 700. Turn the P700 trimpot to the clockwise up to maximum.

3- Adjust R-Y and B-Y outputs to 60mVPP by using P701.

4- Connect a 8K2 resistor between the pins 8 and 16 of IC500 also connect pin 12 to ground.

5- Adjust the color SYNC by using CT700.

6- Delete all modification.

7- Connect osciloscope to the pin 3 of IC700 and adjust the signal level to minimum by using L700 coil. (Bell filter adjustment.)

SIF DETECTOR ADJUSTMENT :

1- Apply 1Khz sound signal with test pattern to RF input.

2- Adjust the maximum sound output by using L208 which is sif detector coil.

3- For D/K sound adjestment , adjust L209 , coil then repeat the A/M steps.

WHITE BALANCE ADJUSTMENT :

1- Apply only white-pattern to RF input and wait 15 minute for heating.

2- Adjust P904, 905, 906 which are RGB bias control trimpots to anti clock-wise at reaside.

3- Adjust P902, and 903 which are G, B driver trimpot to middle level.

4- Adjust brightness, contrast and color to min.

5- Turn the screen voltage trimpot on the EHT transformer to clock-wise until appear any visible picture on the screen.

6- Adjust brightness to 15% dark picture.

7- Adjust the gray level by using P904, 905, 906 an ideal level.

8- Adjust brightness and contrast to max. Than adjust P902 and 903 which are G,B driver trimpots until obtain a white level if appears any color on the screen.

POWER SUPPLY

TEA2019

CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

- DIRECT DRIVE OF THE EXTERNAL SWITCHING TRANSISTOR
- POSITIVE AND NEGATIVE OUTPUT CURRENTS UP TO 0.5A
- CURRENT LIMITATION
- TRANSFORMER DEMAGNETIZATION AND POWER TRANSISTOR SATURATION SENSING
- FULL OVERLOAD AND SHORT-CIRCUIT PROTECTION
- PROPORTIONAL BASE CURRENT DRIVING
- LOW STANDBY CURRENT BEFORE STARTING (1.6mA)
- SYNCHRONIZATION CAPABILITY WITH INTERNAL PLL
- THERMAL PROTECTION

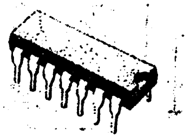
DESCRIPTION

The TEA2019 is an 14-pin mini-dip low cost integrated circuit designed for the control of switch mode power supplies. It has the same basic functions as the TEA2018A but with synchronization capability by internal PLL. It is particularly suitable for applications where oscillator synchronization is required.

Due to its current mode regulation, the TEA2019 facilitates design of power supplies with following features :

- High stability regulation loop.
- Automatic input voltage feed-forward in discontinuous mode fly-back.
- Automatic pulse-by-pulse current limitation.

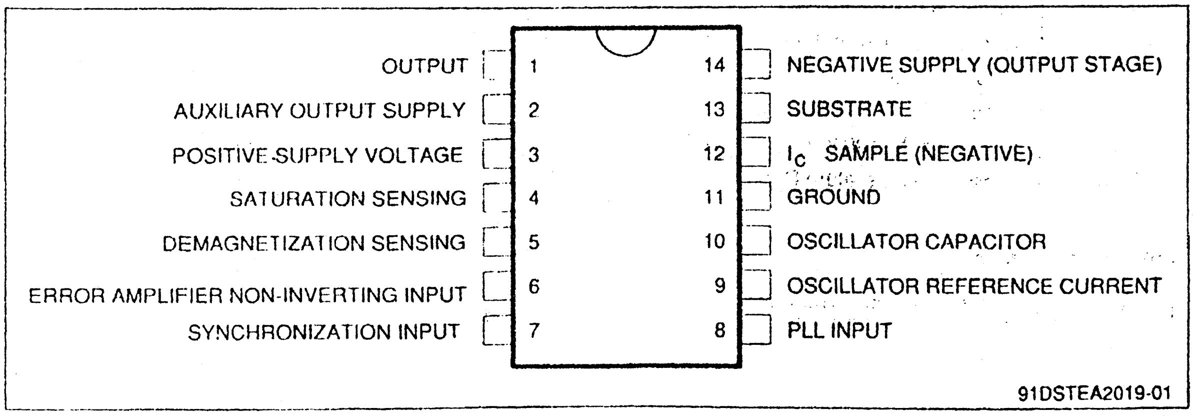
Typical applications : Video Display Units, TV sets, typewriters, micro-computers and industrial applications. For more details, see application note AN406/0591.



DIP 14
(Plastic package)

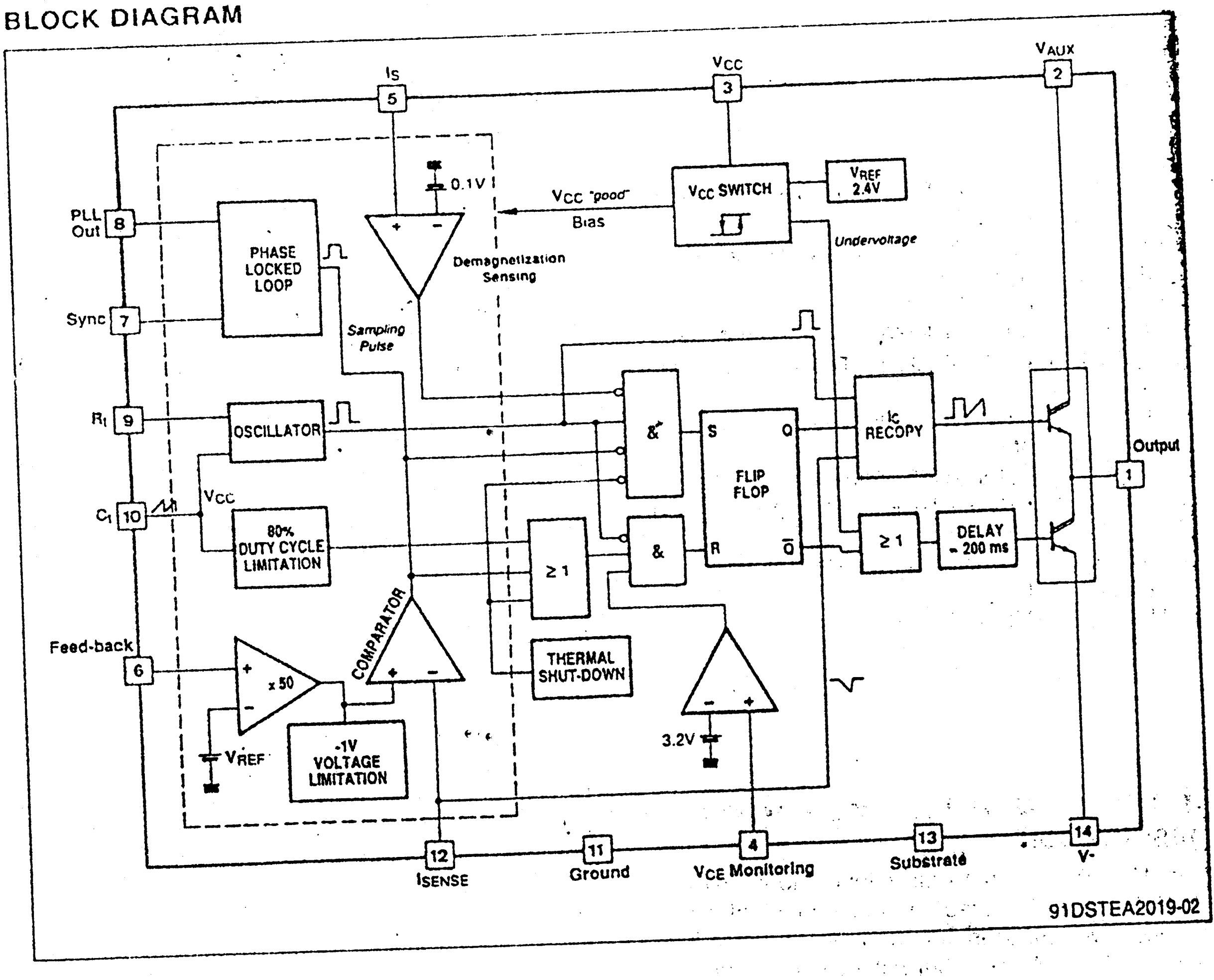
ORDER CODE : TEA2019

PIN CONNECTIONS


OUTPUT
1
AUXILIARY OUTPUT SUPPLY
2
POSITIVE SUPPLY VOLTAGE
3
SATURATION SENSING
4
DEMAGNETIZATION SENSING
5
ERROR AMPLIFIER NON-INVERTING INPUT
6
SYNCHRONIZATION INPUT
7
14
NEGATIVE SUPPLY (OUTPUT STAGE)
13
SUBSTRATE
12
I_C SAMPLE (NEGATIVE)
11
GROUND
10
OSCILLATOR CAPACITOR
9
OSCILLATOR REFERENCE CURRENT
8
PLL INPUT
91DSTEA2019-01

TEA2019

BLOCK DIAGRAM


IS
5
VCC
3
VAUX
2
0.1V
VCC "good"
Bias
VCC SWITCH
VREF 2.4V
Undervoltage
PLL Out
8
PHASE LOCKED LOOP
Demagnetization Sensing
Sync
7
Sampling Pulse
Rt
9
OSCILLATOR
&
S
Q
FLIP FLOP
R
Q̄
Ic RECOPY
Output
1
Ct
10
VCC
80% DUTY CYCLE LIMITATION
≥1
&
≥1
DELAY ≈ 200 ms
COMPARATOR
Feed-back
6
x 50
THERMAL SHUT-DOWN
VREF
-1V VOLTAGE LIMITATION
3.2V
12
ISENSE
11
Ground
4
VCE Monitoring
13
Substrate
14
V-
91DSTEA2019-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^{+}_{CC}	Positive Supply Voltage	15	V
$V_{(aux)}$	Auxiliary Output Supply Voltage	15	V
V^{-}_{CC}	Negative Supply Voltage	– 5	V
I_O (peak)	Peak Output Current (duty cycle < 5%)	± 1	A
I_I	Input Current Pins 4-5	± 5	mA
T_j	Junction Temperature	150	°C
T_{oper}	Operating Ambient Temperature Range	– 20, + 70	°C
T_{stg}	Storage Temperature Range	– 40, + 150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, potentials referenced to ground (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^{+}_{CC}	Positive Supply Voltage	6.6	8	15	V
V_{CC}	Negative Supply Voltage	–1	–3	–5	V
$V_{CC(start)}$	Minimum positive supply voltage required for starting (V^{+}_{CC} rising)		6	6.6	V
$V_{CC(stop)}$	Minimum positive voltage below which device stops operating (V^{+}_{CC} falling)	4.2	4.9	5.6	V
ΔV^{+}_{CC}	Hysteresis on V^{+}_{CC} Threshold	0.7	1.1	1.6	V
$I_{CC(sb)}$	Standby Supply Current Before Starting [$V^{+}_{CC} < V_{CC(start)}$]		1	1.6	mA
$V_{th\ (Ic)}$	Current Limitation Threshold Voltage (pin 12)	–1100	–1000	–880	mV
$R_{(Ic)}$	Collector Current Sensing Input Resistance		1000		Ω
I_S	Demagnetization Sensing Threshold	75	100	125	mV
	Demagnetization Sensing Input Current (pin 5 grounded)		1		µA
τ_{max}	Maximum Duty Cycle	70	80		%
A_V	Error Amplifier Gain		50		
I^{+}_{I}	Error Amplifier Input Current (non-inverting input) (pin 6)		2		µA
$V_{(REF)}$	Internal Reference Voltage	2.3	2.4	2.5	V
$\frac{\Delta V_{(REF)}}{\Delta T}$	Reference Voltage Temperature Drift		10^{-4}		V/°C
T_{OSC}	Oscillator Free-running Period (R = 59kΩ, C = 1.5nF)	60	65	70	µs
$\frac{\Delta f_{OSC}}{\Delta T}$	Oscillator Frequency Drift with Temperature (V^{+}_{CC} = + 8V)		0.05		%/°C
$\frac{\Delta f_{OSC}}{\Delta V_{CC}}$	Oscillator Frequency Drift with V^{+}_{CC} (+ 8V < V^{+}_{CC} < + 14V)		0.5		%/V
t_{on}(min)	Minimum Conducting Time (C_t = 1nF)		2		µs

TAB-03

SYNCHRONIZATION INPUT (pin 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{7pp}	Peak to Peak Sawtooth Voltage		0.5	2.5	V
$R_{(7)}$	Input Impedance		20		kΩ

TAB-04

PLL CHARACTERISTICS (see Test Circuit)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frequency Sensitivity		100		Hz/µA
ΔT	Capture Range (T_{OSC} = 64µs Typ.) $T_{OSC} - T_{SYN\ min}$ $T_{SYN\ max} - T_{OSC}$	5.5 4.5	8 8		µs µs

TAB-05

SATURATION SENSING (pin 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{(4)}$	Input Threshold		3.2		V
$I_{(4)}$	Input Current (V_4 > 3.2V)	50			µA
	Input Internal Resistance		1		kΩ

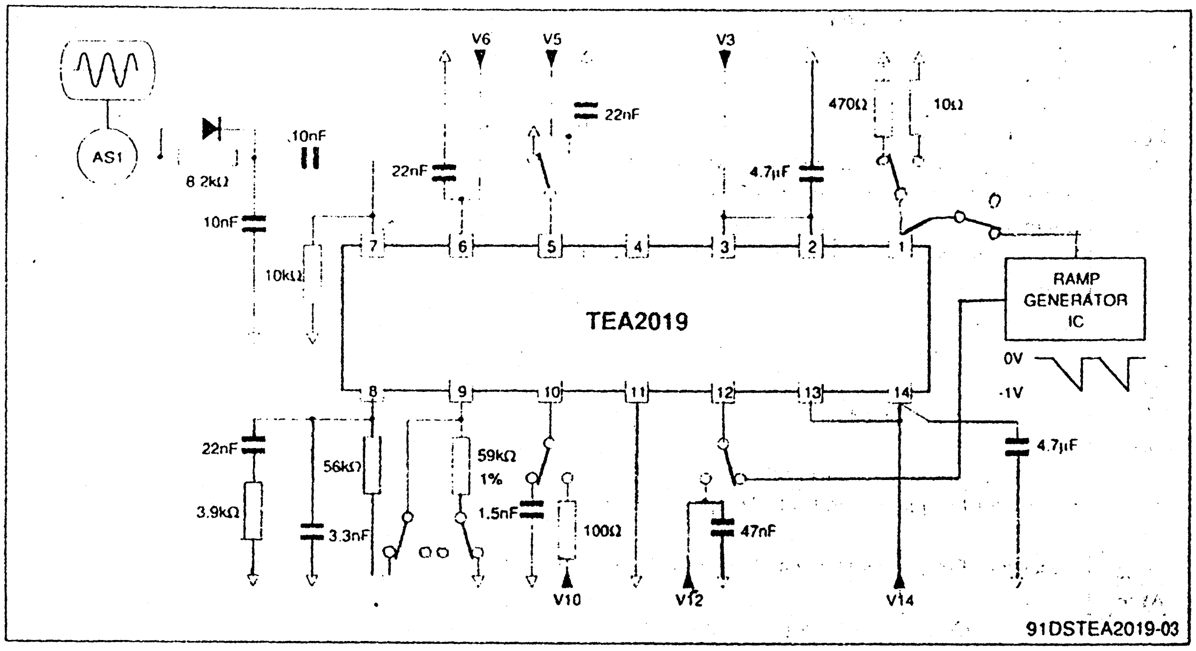
TAB-06

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^{+}_{CC}	Positive Supply Voltage		8		V
V_{CC}	Negative Supply Voltage		3		V
I_O	Output Current			0.5	A
F_{oper}	Operating Frequency		30		kHz

TAB-07

TYPICAL CIRCUIT


AS1
8.2kΩ
10nF
10nF
10kΩ
22nF
V6
V5
22nF
V3
4.7µF
470Ω
10Ω
TEA2019
1
2
3
4
5
6
7
8
9
10
11
12
13
14
RAMP GENERATOR IC
0V
-1V
4.7µF
22nF
3.9kΩ
3.3nF
56kΩ
59kΩ 1%
1.5nF
100Ω
47nF
V10
V12
V14
91DSTEA2019-03

GENERAL DESCRIPTION (see application note AN406/0591)

OPERATING PRINCIPLES (figure)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator saw-tooth which acts as clock signal. The period T_{osc} is given by : $T_{osc} \approx 0.69\ C_t\ (R_t + 2000)$

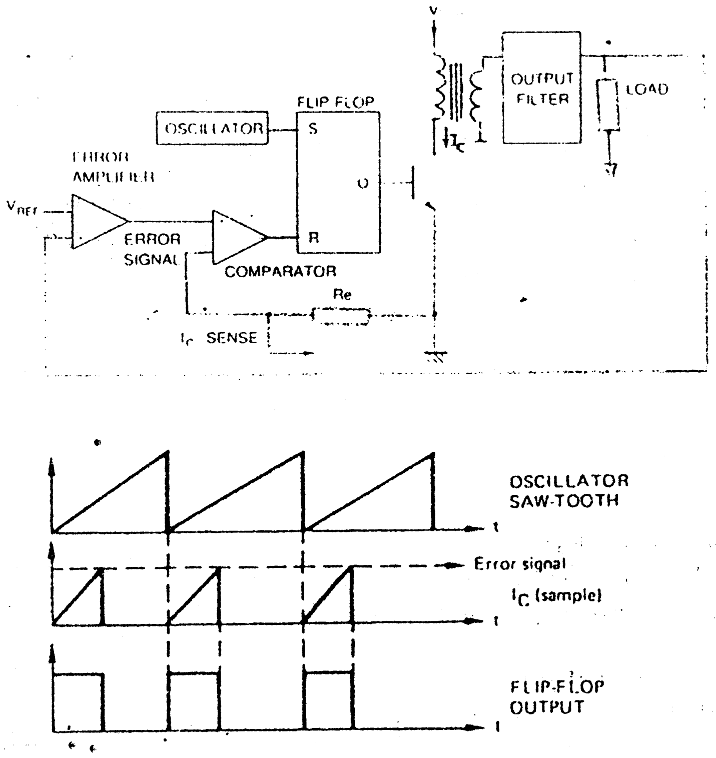
(T_{osc} in seconds, C_t in Farad, R_t in Ohm)

The end of the conduction time is determined by a signal issued from comparing the following signals.

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor.

b) the output of the error amplifier.

Figure 1 : Current Mode Control.



91DSTEA2019-04

89DSTEA2019-05

BASE DRIVE

- **Fast turn-on**

On each period, a current pulse ensures fast transistor switch-on.

This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.

- **Proportional base drive**

In order to save power, the positive base current after the starting pulse becomes an image of the collector current.

The ratio $\frac{I_C}{I_B}$ is programmed as follows (figure 2).

$$\frac{I_C}{I_B} = \frac{R_B}{R_E}$$

- **Efficient and fast switch-off**

When the positive base drive is removed, 1s (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

SAFETY FUNCTIONS

- **Overload & short-circuit protection**

When the voltage applied to pin 12 exceeds the current limitation thershold voltage [$V_{th(Ic)}$], the output flip-flop is reset and the transistor is turned off.

The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 12 at the maximum allowable collector current.

- **Demagnetization sensing**

This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.

When not used, pin 5 must be grounded.

- $t_{on(max)}$

Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70% of the period.

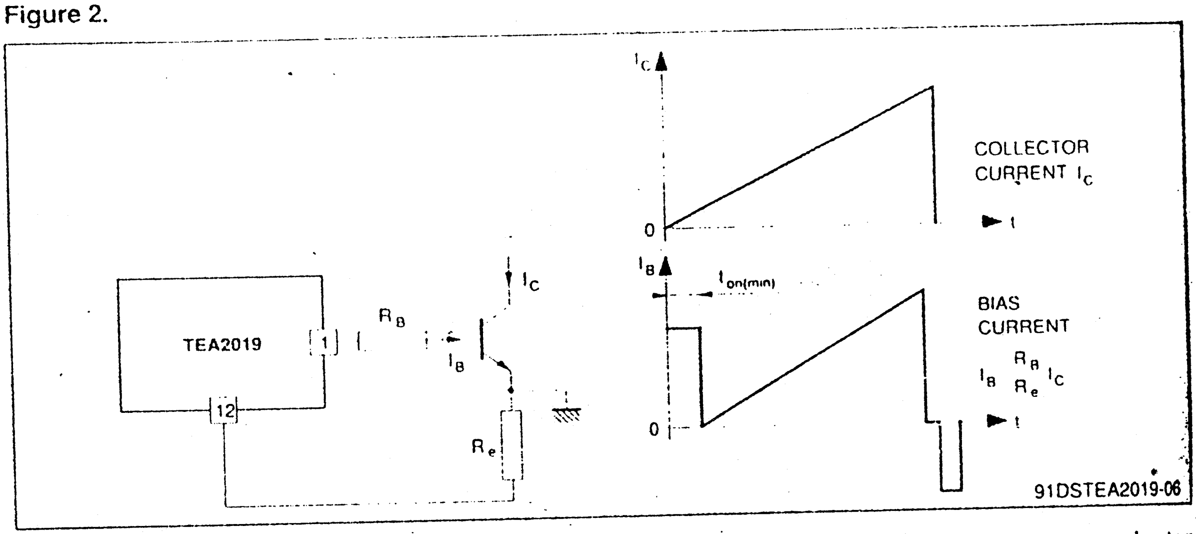
- $t_{on(min)}$

A minimum conducting time is ensured during each period (see figure 2).

- **Supply voltage monitoring**

The TEA2019 will stop operating if V_{CC+} on pin 3 falls below the threshold level $V_{CC(stop)}$.

Figure 2.



STARTING PROCESS (figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.

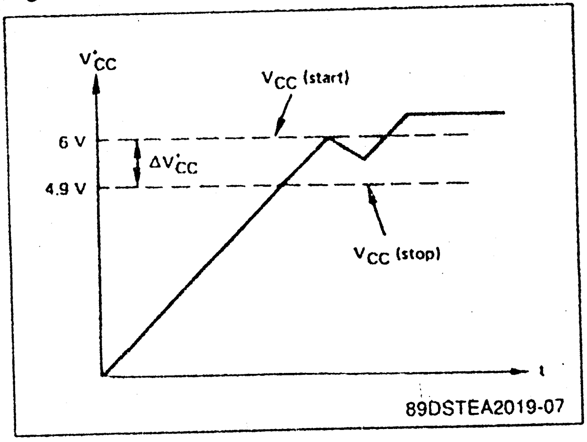
This current charges the power supply storage capacitor of the device.

No output pulses are available before the voltage on pin 3 has reached the threshold level [$V_{CC(start)}$, V^{+}_{CC} rising].

During this time the TEA2019 draws only 1 mA (typically). When the voltage on pin 3 reaches this threshold base drive pulses appear.

The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1V (typically) (Δ Vcc) is implemented to avoid the device from stopping.

Figure 3 : Normal TEA2019 Start up Sequence.

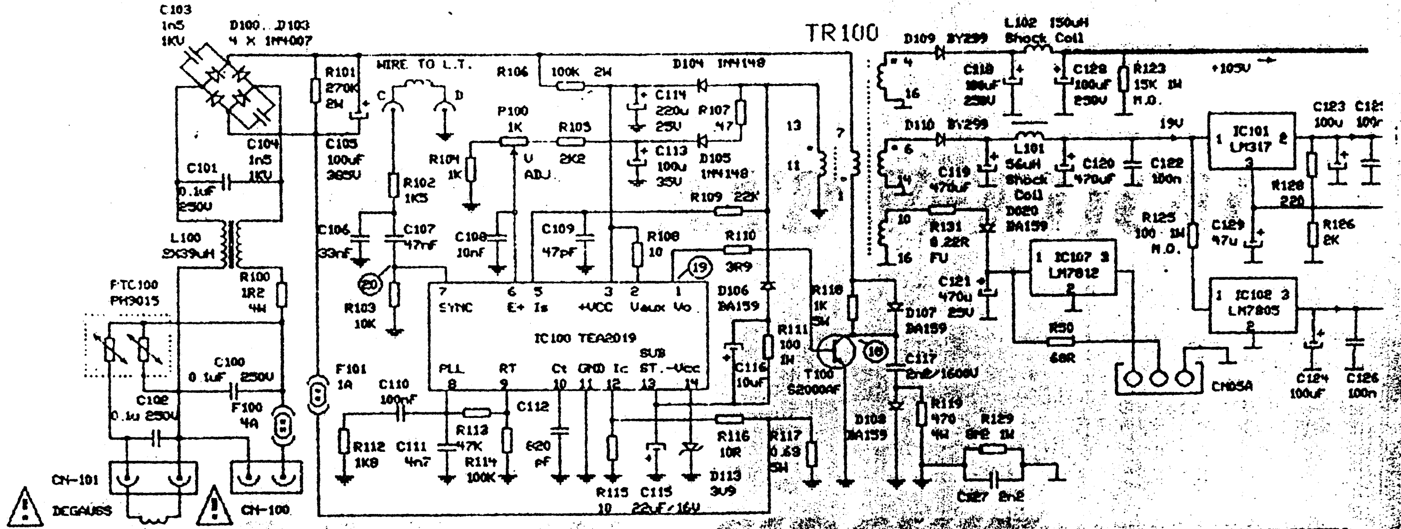


The TEA2019 has some additional capabilities compared to the TEA2018A :

- The oscillator charge current its supplied through an internal current generator, programmed externally - instead of using an external charging resistor. The sawtooth so obtained is linear.
- The oscillator can be synchronized through an internal PLL circuit. This feature provides synchronization between the external sync pulse and the end of the switching transistor current. The sync pulse can be for example the fly-back pulse of a TV horizontal sweep circuit. As indicated in the application diagram, this pulse is applied first to a R.C. network to obtain a low voltage sawtooth and then to pin 7 of the circuit. The PLL output (pin 8) supplies a correction current to pin 9 through an external resistor, so as to maintain the oscillator at the correct frequency (refer to application note AN406/0591 for detailed information).
- In the TEA2019, the power supply of the positive output stage is separated from the main power supply, so that it can be supplied from a lower voltage in order to reduce the I.C. power dissipation.
  For low power applications, the circuit can be normally supplied by connecting pins 2 and 3 together.
- In order to protect the substrate (pin 13) from the parasitic voltage peaks produced by negative output current peaks at pin 14, the substrate (pin 13) is internally separated from the negative supply (pin 14). They must be externally connected together.
- The switching transistor saturation voltage can be monitored at pin 4. To achieve this, a high voltage diode must be connected between the collector of the switching transistor and pin 4. Also a resistor must be connected from pin 4 to V^{+}_{CC}

(see application diagram). This arrangement is useful when the chosen value of base current is very low and as a consequence the saturation voltage will be high. In this event, when $V_{CE(sat)}$ increases above 2.5V, the base current is interrupted before the normal end of the period.
Remark : the TEA2019 can also operate without this protection.

TYPICAL APPLICATION


C103 1n5 1KV
D100...D103 4 X 1N4007
R101 270K 2W
WIRE TO L.T.
C
D
R106
100K 2W
D104 1N4148
P100 1K
R105 2K2
C114 220u 25V
R107 .47
C113 100u 35V
D105 1N4148
R104 1K
V ADJ
C104 1n5 1KV
C105 100uF 385V
C101 0.1uF 250V
R102 1K5
R109 22K
L100 2X39uH
C106 33nF
C107 47nF
C108 10nF
C109 47pF
R108 10
R110 3R9
R100 1R2 4W
FTC100 PH9015
R103 10K
7 SYNC
6 E+
5 Is
3 +VCC
2 Vaux
1 Vo
IC100 TEA2019
PLL 8
RT 9
Ct 10
GND 11
Ic 12
SUB ST. 13
-Vcc 14
D106 BA159
R118 1K 5W
R111 100 1W
C116 10uF
T100 S2000AF
C100 0.1uF 250V
C102 0.1u 250V
F100 4A
F101 1A
C110 100nF
C112
R112 1K8
C111 4n7
R113 47K
R114 100K
820 pF
R116 10R
R117 0.68 5W
D113 3V9
R115 10
C115 22uF/16V
CN-101
DEGAUSS
CN-100
TR100
13
11
7
1
D109 BY299
L102 150uH Shock Coil
4
16
C118 100uF 250V
C128 100uF 250V
R123 15K 1W N.O.
+105V
D110 BY299
6
14
C119 470uF
L101 56uH Shock Coil
C120 470uF
C122 100n
19V
IC101 LM317
C123 100u
R128 220
R126 2K
C129 47u
R125 100 1W N.O.
10
R131 0.22R FU
D020 BA159
IC107 LM7812
IC102 LM7805
C121 470u 25V
D107 BA159
C117 2n2/1600V
D108 BA159
R119 470 4W
R129 8R2 1W
C127 2n2
R50 68R
CN05A
C124 100uF
C126 100n

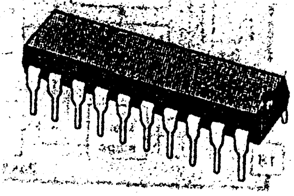
HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

TDA8215A

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE

ADVANCE DATA



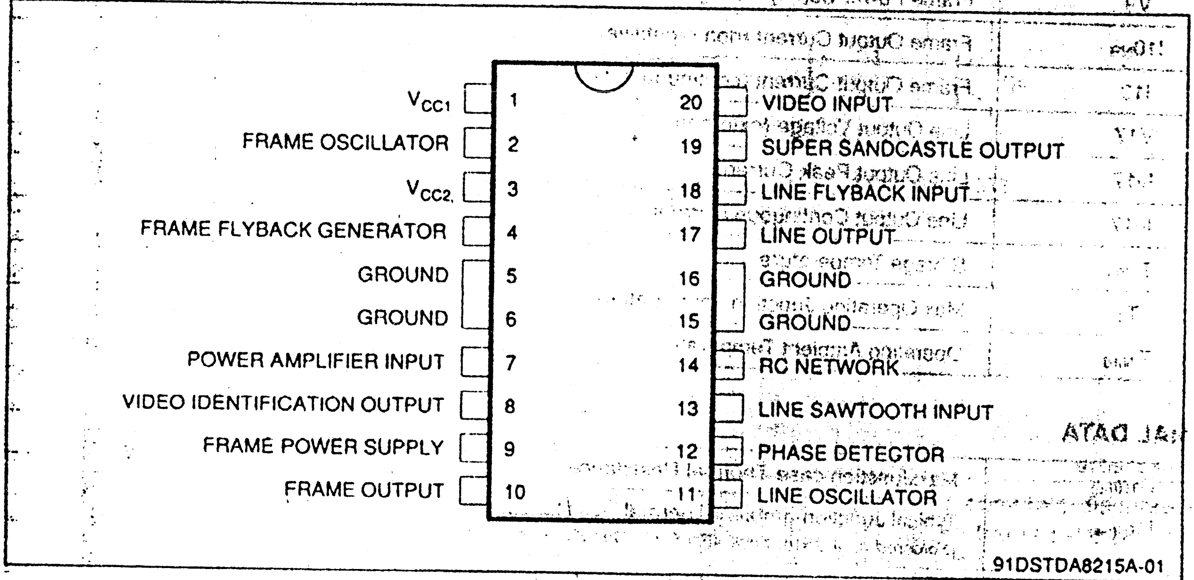
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8215A

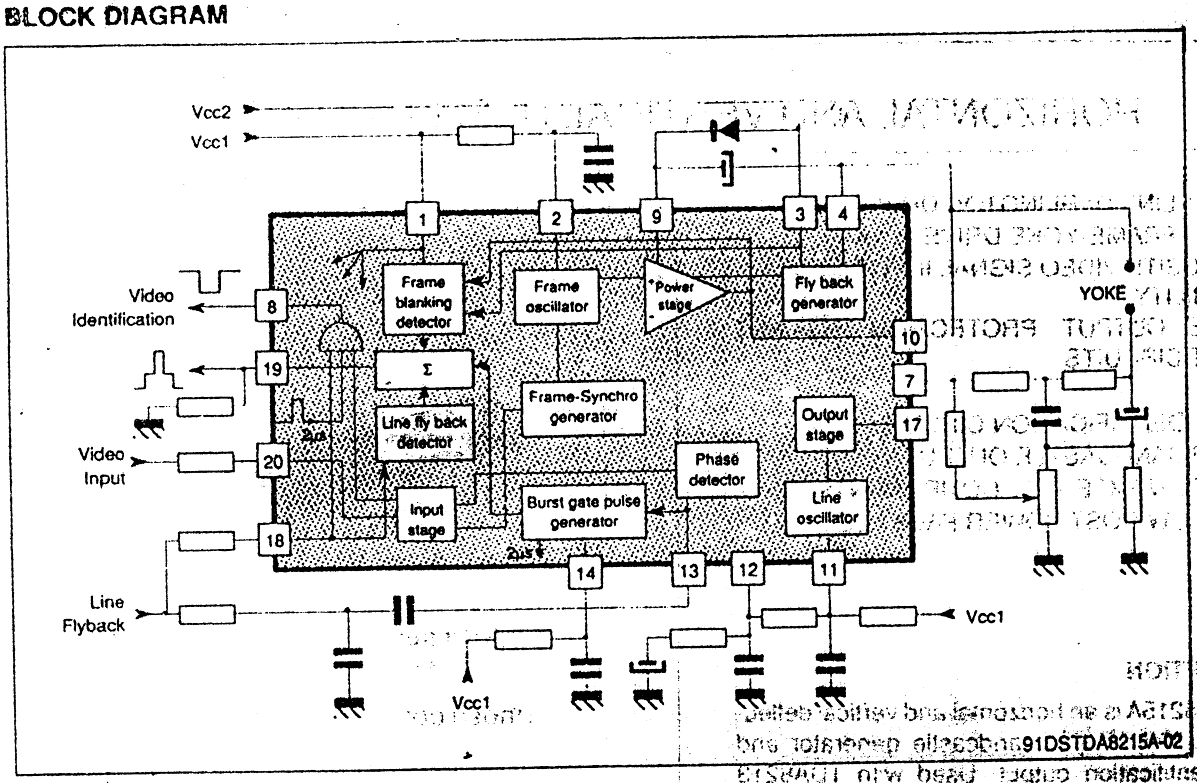
DESCRIPTION

The TDA8215A is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete, low-cost solution for PAL applications. THe TDA8215A has been specially designed for direct drive of line DARLINGTON transistors.

PIN CONNECTIONS


V_{CC1}
1
FRAME OSCILLATOR
2
V_{CC2}
3
FRAME FLYBACK GENERATOR
4
GROUND
5
GROUND
6
POWER AMPLIFIER INPUT
7
VIDEO IDENTIFICATION OUTPUT
8
FRAME POWER SUPPLY
9
FRAME OUTPUT
10
20
VIDEO INPUT
19
SUPER SANDCASTLE OUTPUT
18
LINE FLYBACK INPUT
17
LINE OUTPUT
16
GROUND
15
GROUND
14
RC NETWORK
13
LINE SAWTOOTH INPUT
12
PHASE DETECTOR
11
LINE OSCILLATOR
91DSTDA8215A-01

BLOCK DIAGRAM


Vcc2
Vcc1
1
2
9
3
4
Frame blanking detector
Frame oscillator
Power stage
Fly back generator
YOKE
Video Identification
8
19
Σ
10
7
Frame-Synchro generator
Line fly back detector
Output stage
17
Video Input
20
Phase detector
Input stage
Burst gate pulse generator
Line oscillator
18
14
13
12
11
Line Flyback
Vcc1
Vcc1
91DSTDA8215A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

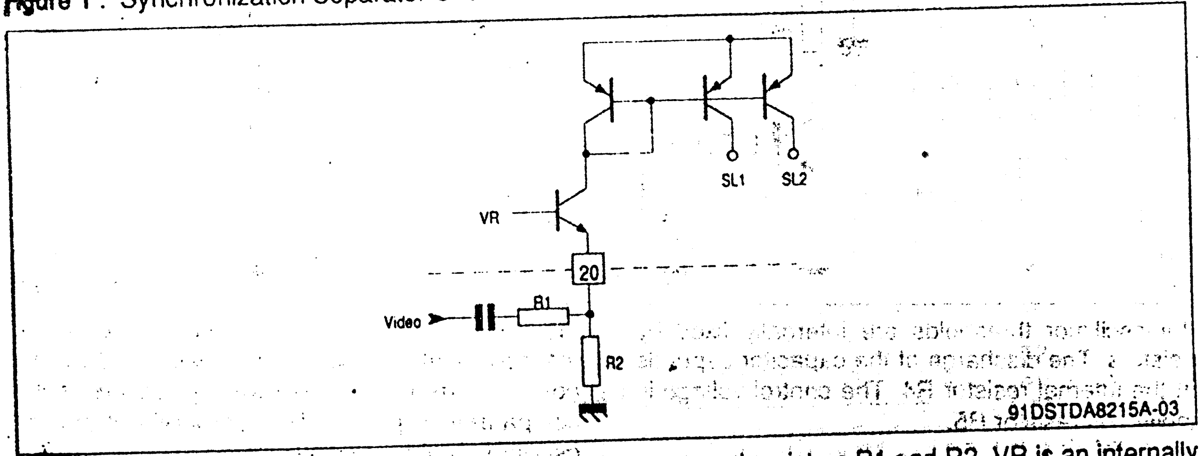
$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35μm thick 45cm² PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

GENERAL DESCRIPTION

The TDA8215A performs all the video and power functions required to provide signals for the line driver and frame yoke.

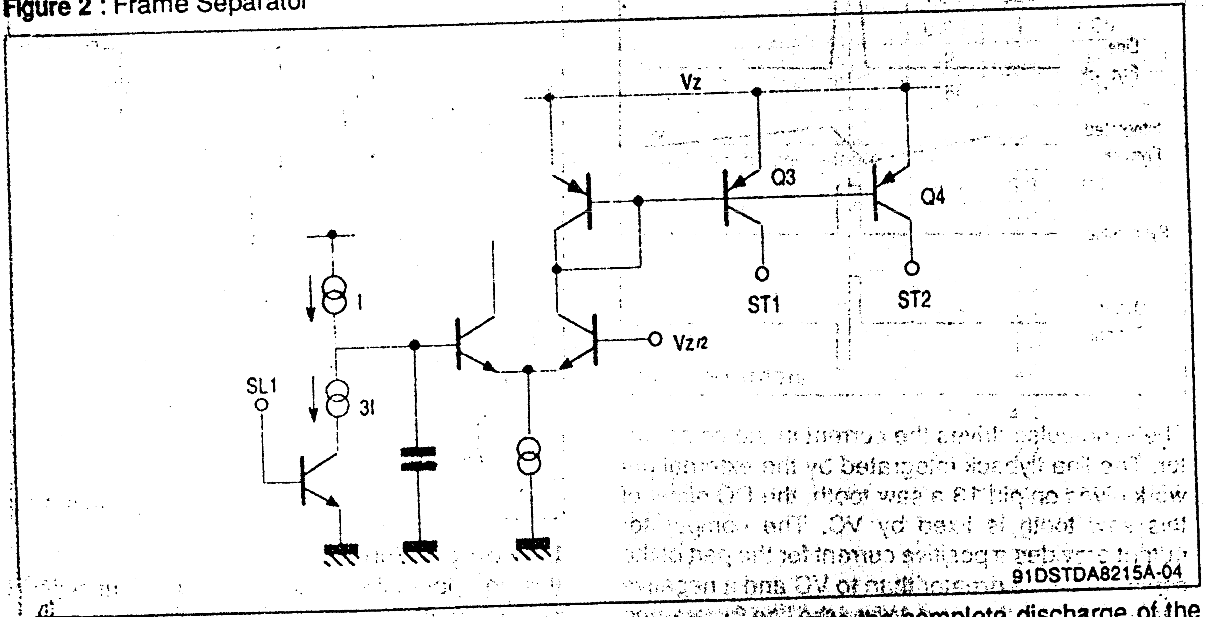
It contains:
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

Figure 1 : Synchronization Separator Circuit



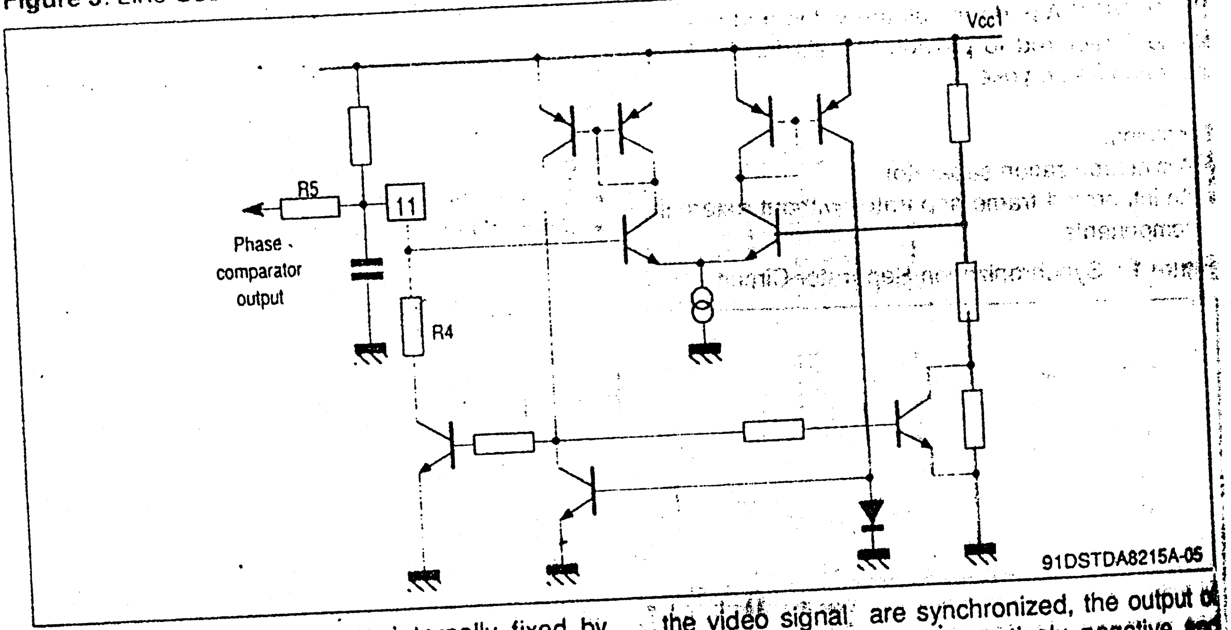
The slice level of sync-separation is fixed by value of the external resistors R1 and R2. VR is an internally fixed voltage.

Figure 2 : Frame Separator



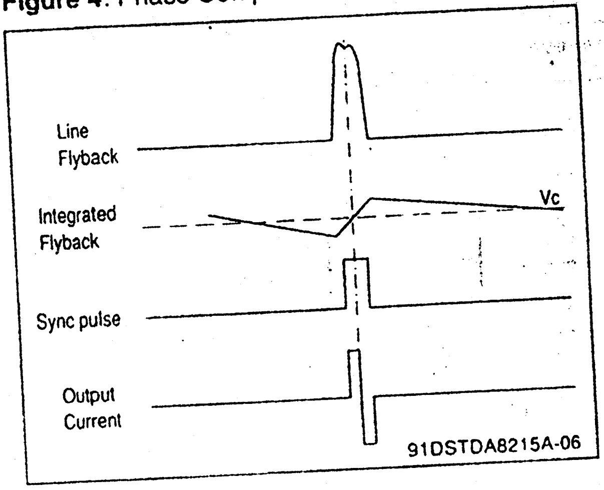
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 3: Line Oscillator


Vcc1
R5
11
Phase comparator output
R4
91DSTDA8215A-05

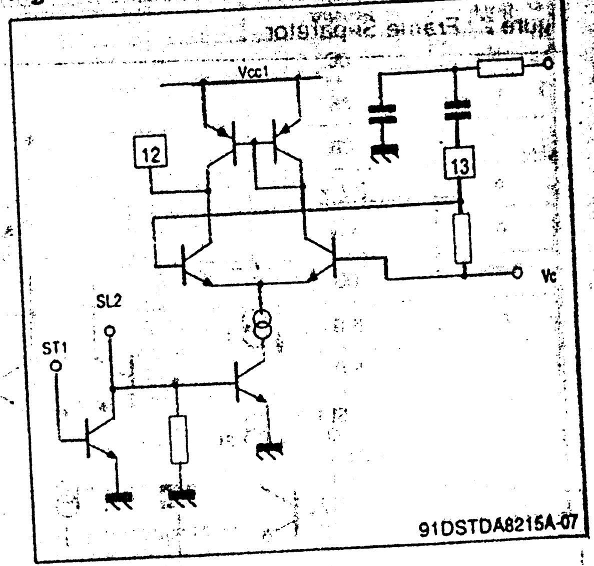
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4: Phase Comparator


Line Flyback
Integrated Flyback
Vc
Sync pulse
Output Current
91DSTDA8215A-06

The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator, to prevent frequency drift of the line oscillator on the frame beginning.

Figure 5


Vcc1
12
13
Vc
SL2
ST1
91DSTDA8215A-07

Line output (Pin 17)

It is an open-collector output. The output negative pulse time is 22µs for a 64µs period.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I20 = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 800mA during 2µs)		2.2		V
OPW	Output Pulse width (line period = 64µs , negative pulse)	19	21	23	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control Voltage Range	2.60		7.10	V
VIDEO IDENTIFICATION (Pin 8)					
	Low Level Output when the line synchro tip is centered in the line retrace				
V_{H8}	without Video Signal (I_8 = -500µA)	4.5	6.3	0.9	V
V_{L8}	with Video Signal (I_8 = 50µA)		0.6	0.9	V
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C

ELECTRICAL CHARACTERISTICS (continued)

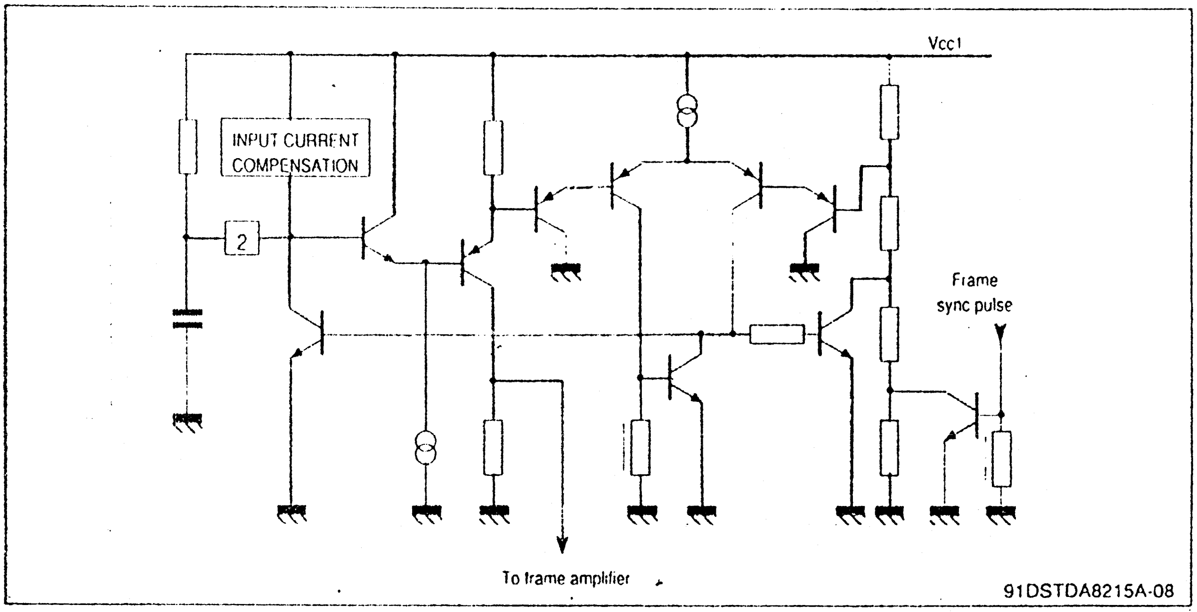
V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
$V_{CC}2$	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Votage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V4/3 with				
F2DA	$I_{4 \to 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4 \to 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V3/4 with				
FSVA	$I_{3 \to 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3 \to 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	4 Note 1	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 2)		6		µs

Notes :

1. Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is $V_{CC2} - 2V_{BE}$ the other input of the comparator is tied to the frame amplifier output. Application circuit uses the frame flyback generator.
2. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse also the duration of the burst key pulse.

Figure 6: Frame Oscillator

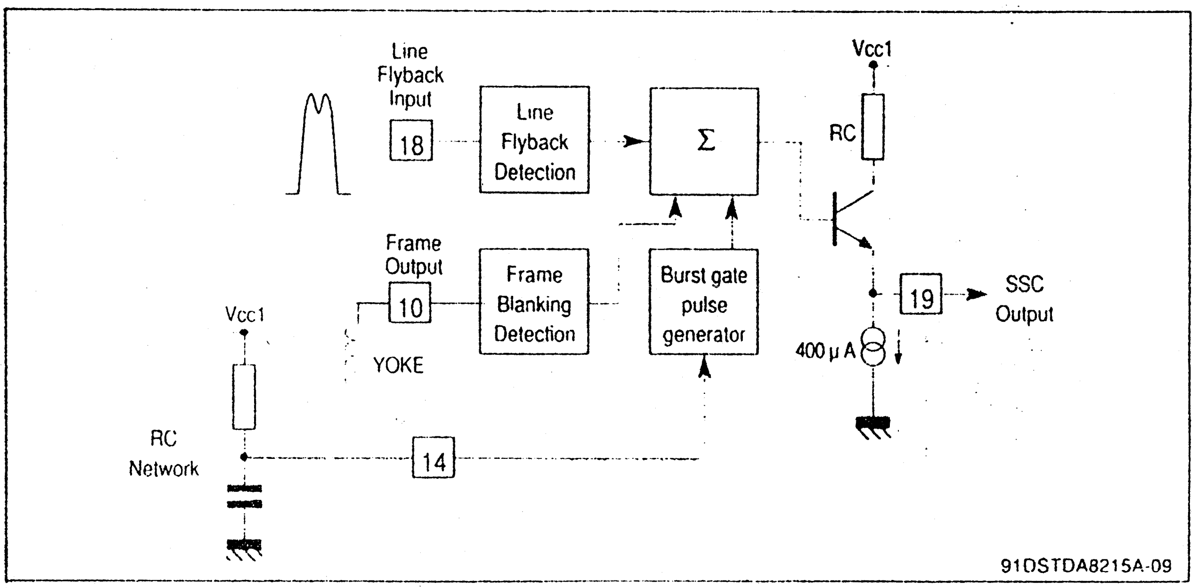

Vcc1
INPUT CURRENT COMPENSATION
2
Frame sync pulse
To frame amplifier
91DSTDA8215A-08

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame output amplifier

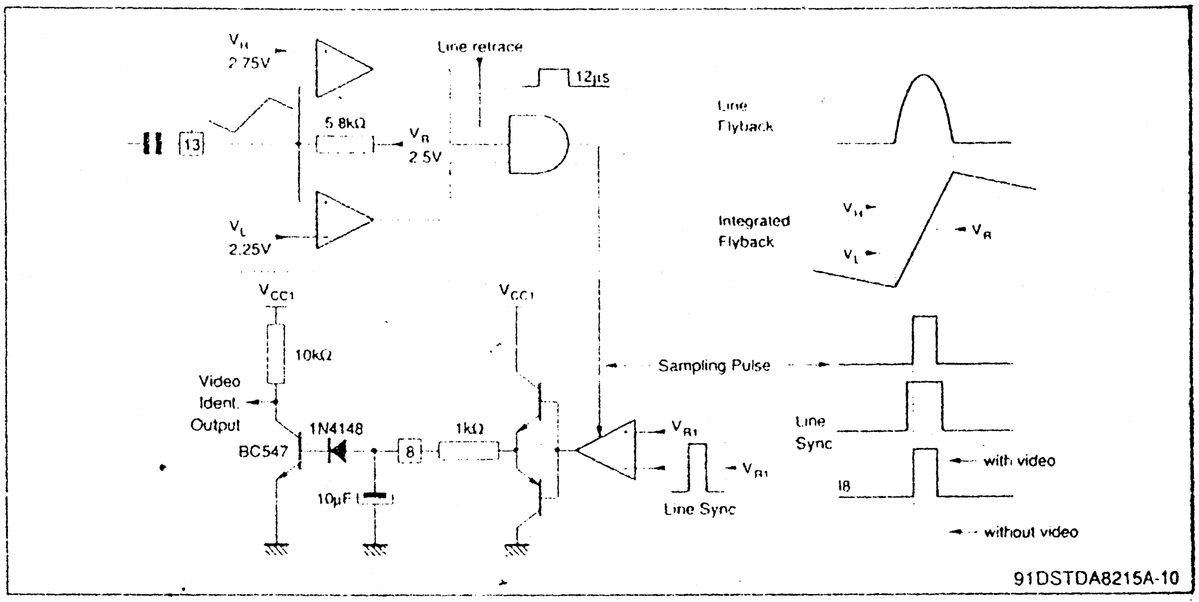
This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

Figure 7: Super sandcastle generator


Line Flyback Input
18
Line Flyback Detection
Σ
Vcc1
RC
Frame Output
10
Frame Blanking Detection
Burst gate pulse generator
19
SSC Output
Vcc1
YOKE
400 µ A
RC Network
14
91DSTDA8215A-09

The frame blanking is detected by the frame flyback generator. When the output voltage of the frame amplifier exceeds $V_{CC}2$-$2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (pin 14). It is referenced to the middle of the line flyback.

Figure 8 : Video Identification Circuit (Pin 8).


V_H 2.75V
V_L 2.25V
13
5.8kΩ
V_R 2.5V
Line retrace
12µs
Line Flyback
Integrated Flyback
V_H
V_L
V_R
V_{CC1}
V_{CC1}
10kΩ
Video Ident. Output
BC547
1N4148
8
1kΩ
10µF
V_{R1}
V_{R1}
Line Sync
Sampling Pulse
Line Sync
18
with video
without video

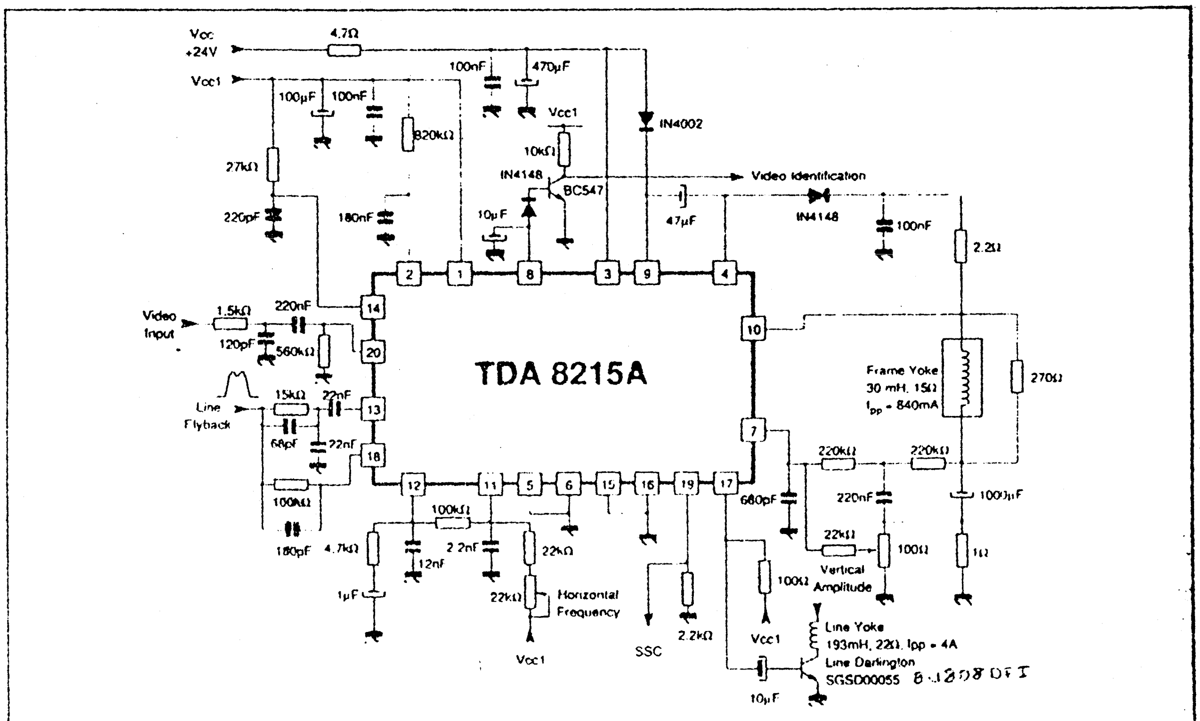
91DSTDA8215A-10

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs sampling pulse. This 2µs pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark : minimum saw-tooth amplitude on Pin 13 has to be 2VPP (typ. : 2.5VPP).

TYPICAL APPLICATION

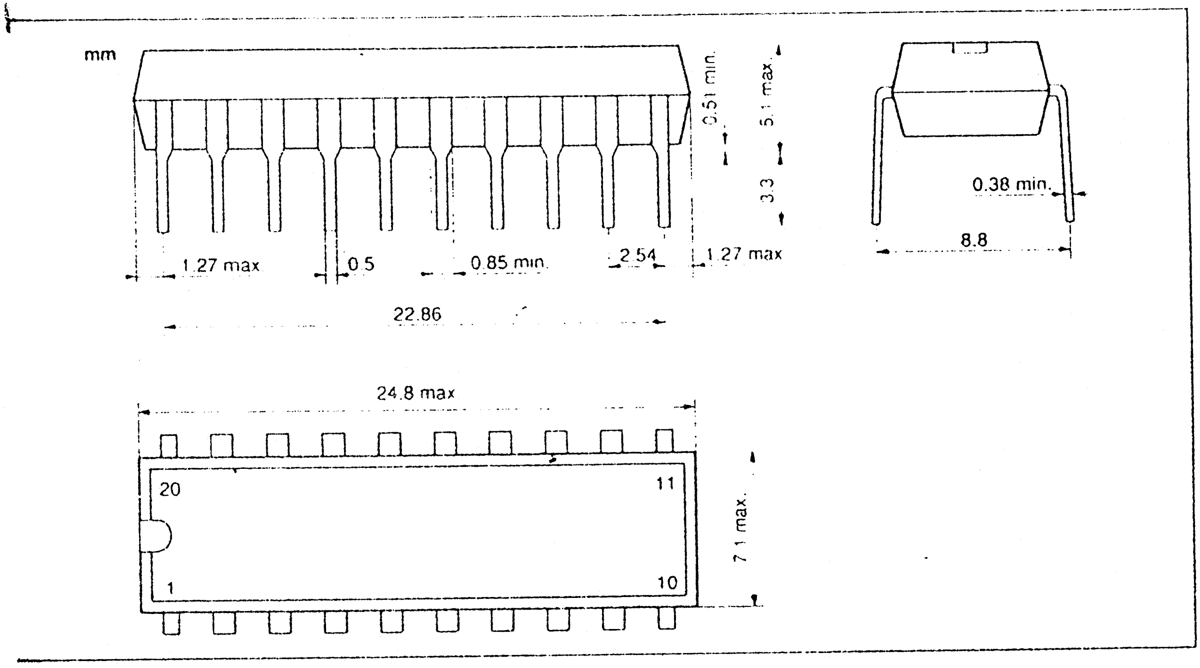

Vcc +24V
Vcc1
4.7Ω
100nF
470µF
100µF
100nF
820kΩ
Vcc1
1N4002
27kΩ
10kΩ
1N4148
BC547
Video identification
220pF
180nF
10µF
47µF
1N4148
100nF
2.2Ω
Video Input
1.5kΩ
220nF
120pF
560kΩ
TDA 8215A
Frame Yoke 30 mH, 15Ω I_{pp} = 840mA
270Ω
Line Flyback
15kΩ
22nF
68pF
22nF
100kΩ
180pF
4.7kΩ
1µF
100kΩ
2.2nF
12nF
22kΩ
22kΩ
Horizontal Frequency
Vcc1
SSC
2.2kΩ
Vcc1
680pF
220nF
220kΩ
220kΩ
100µF
22kΩ
100Ω
100Ω
1Ω
Vertical Amplitude
Line Yoke 193mH, 22Ω, Ipp = 4A
Line Darlington SGSD00055
10µF
2
1
8
3
9
4
14
20
13
18
10
7
12
11
5
6
15
16
19
17

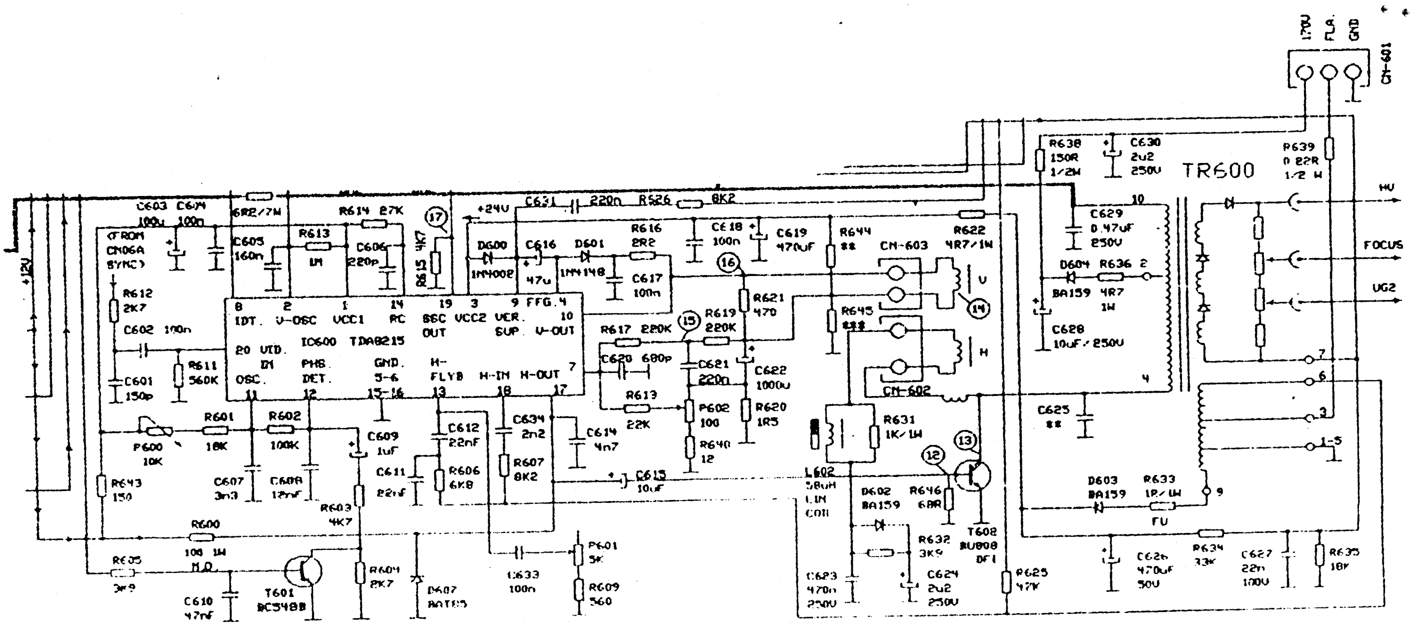
Note : Pins 5 - 6 : Frame oscillator ground
Pins 15 - 16 : Frame and line power ground

91DSTDA8215A-11

PACKAGE MECHANICAL DATA

20 PINS - POWER DIP 16 + 2 + 2


mm
0.51 min.
5.1 max.
3.3
0.38 min.
8.8
1.27 max
0.5
0.85 min.
2.54
1.27 max
22.86
24.8 max
20
11
1
10
7.1 max.

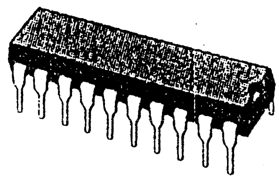

170V
FLA.
GND
CN-601
+12V
C603 100u
C604 100n
6R2/7W
R614 27K
(FROM CN06A SYNC)
C605 160n
R613 1M
C606 220p
R615 4K7
⑰
+24V
C631 220n
R526 8K2
D600 1N4002
C616 47u
D601 1N4148
R616 2R2
C617 100n
C618 100n
C619 470uF
R644 **
R622 4R7/1W
CN-603
⑯
⑭
V
H
R612 2K7
C602 100n
C601 150p
R611 560K
8 IDT.
2 V-OSC
1 VCC1
14 RC
19 SSC OUT
3 VCC2
9 VER. SUP.
FFG.4
10 V-OUT
20 VID. IN
IC600 TDA8215
OSC. 11
PHS. DET. 12
GND. 5-6 15-16
H-FLYB 13
H-IN 18
H-OUT 17
7
R617 220K
⑮
R619 220K
R621 470
R645 ***
C620 680p
C621 220n
C622 1000u
R613 22K
P602 100
R620 1R5
R640 12
CN-602
R631 1K/1W
⑫
⑬
P600 10K
R601 10K
R602 100K
C609 1uF
C612 22nF
C634 2n2
C614 4n7
C611 22nF
R606 6K8
R607 8K2
C615 10uF
L602 58uH LIN COIL
D602 BA159
R646 68R
T602 BU808 DFI
R643 150
C607 3n3
C608 12nF
R603 4K7
R600 100 1W M.O.
R605 3K9
C610 47nF
T601 BC548B
R604 2K7
D607 BAT85
C633 100n
P601 5K
R609 560
R632 3K9
C623 470n 250V
C624 2u2 250V
R625 47K
R638 150R 1/2W
C630 2u2 250V
TR600
R639 0.22R 1/2 W
C629 0.47uF 250V
D604 BA159
R636 4R7 1W
C628 10uF/250V
C625 **
10
2
4
7
6
3
1-5
9
HV
FOCUS
VG2
D603 BA159
R633 1R/1W
FU
C626 470uF 50V
R634 33K
C627 22n 100V
R635 10K

PAL DECODER AND VIDEO PROCESSOR CIRCUIT

TDA8217

PAL DECODER AND VIDEO PROCESSOR

- RGB OUTPUTS
- SINGLE CHIP CHROMA AND LUMINANCE PROCESSOR
- DC CONTROL BRIGHTNESS, CONTRAST, AND SATURATION
- FEW EXTERNAL COMPONENTS
- FAST BLANKING INPUT FOR OSD INSERTION
- SUPER SANDCASTLE INPUT



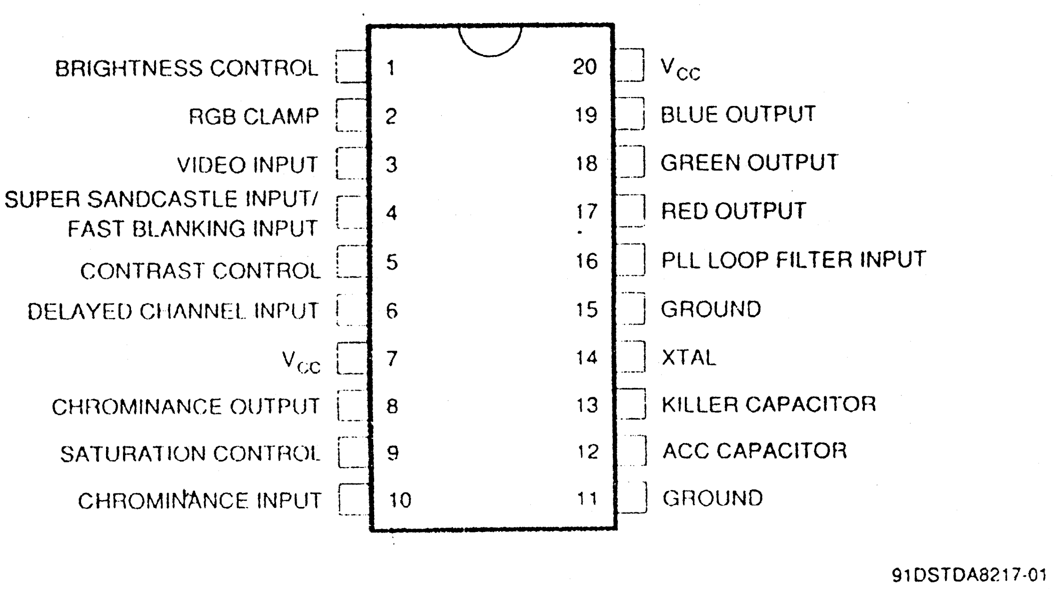
DIP20
(Plastic Package)

ORDER CODE : TDA8217

DESCRIPTION

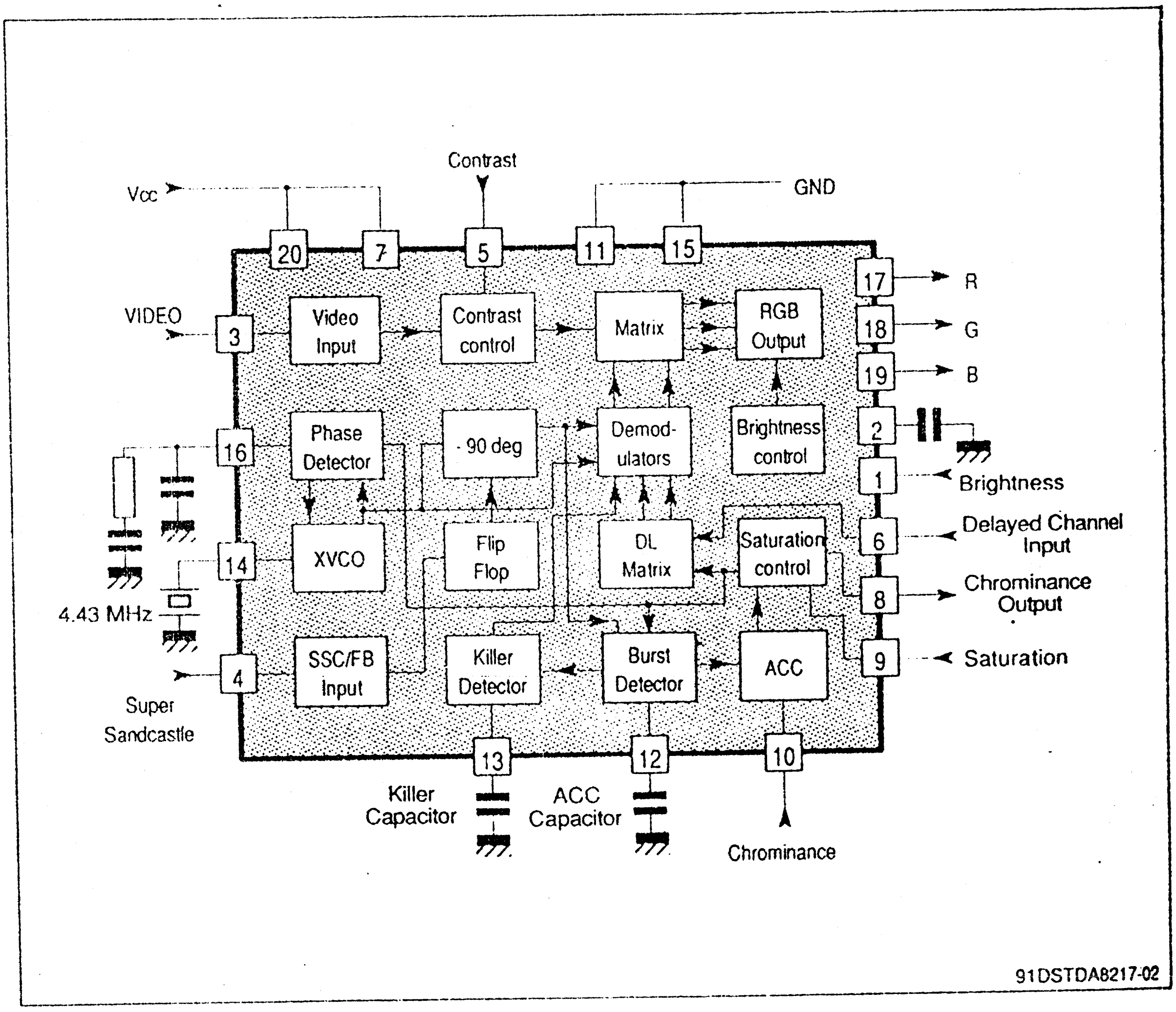
The TDA8217 is a monolithic integrated color decoder for the PAL standard. It includes in a 20 pins IC all the functions required for the identification and demodulation of PAL signals, and all the videoprocessor functions up to the drive of the video stages. Used with TDA8213 (video & sound system) and TDA8214A (H/V deflection circuit), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS


BRIGHTNESS CONTROL 1
RGB CLAMP 2
VIDEO INPUT 3
SUPER SANDCASTLE INPUT/ FAST BLANKING INPUT 4
CONTRAST CONTROL 5
DELAYED CHANNEL INPUT 6
V_{CC} 7
CHROMINANCE OUTPUT 8
SATURATION CONTROL 9
CHROMINANCE INPUT 10
20 V_{CC}
19 BLUE OUTPUT
18 GREEN OUTPUT
17 RED OUTPUT
16 PLL LOOP FILTER INPUT
15 GROUND
14 XTAL
13 KILLER CAPACITOR
12 ACC CAPACITOR
11 GROUND
91DSTDA8217-01

TDA8217

BLOCK DIAGRAM


Contrast
Vcc
GND
20
7
5
11
15
VIDEO
3
Video Input
Contrast control
Matrix
RGB Output
17
18
19
R
G
B
16
Phase Detector
- 90 deg
Demod-ulators
Brightness control
2
1
Brightness
XVCO
Flip Flop
DL Matrix
Saturation control
6
Delayed Channel Input
14
4.43 MHz
8
Chrominance Output
4
SSC/FB Input
Killer Detector
Burst Detector
ACC
9
Saturation
Super Sandcastle
13
12
10
Killer Capacitor
ACC Capacitor
Chrominance
91DSTDA8217-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	12	V
T_{OPER}	Operating temperature	0 , + 70	°C
T_{STG}	Storage temperature	-55 , + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH\ (j-a)}$	Junction to ambient thermal resistance	Max.	80	°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

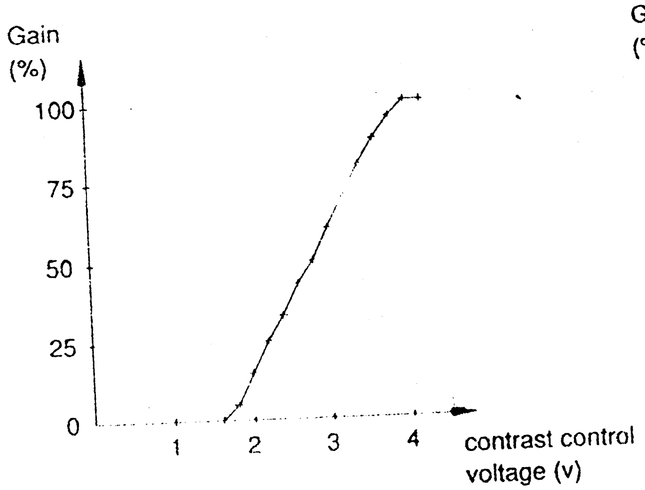
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		8	9	10	V
I_{CC}	Supply Current	No Load		30	50	mA
P_D	Total Power Dissipation	No Load		270	450	mW
LUMINANCE INPUT (Pin 3)						
	Input Level before Clipping (Black to White)				500	mV$_{PP}$
	DC Operating Voltage	No Input Signal	2.5	2.8	3.1	V
	Input Current	• During Burst Period • Out of Burst Period	± 50	± 100	± 150 5	µA µA
CHROMINANCE INPUT (Pin 10)						
	Input Level before Clipping				900	mV$_{PP}$
	Minimum Burst Signal Amplitude within the ACC Control Range		30			mV$_{PP}$
	ACC Control Range	Change of Burst Signal over whole ACC Control Range < 1dB	30			dB
	Input Impedance		6	8	12	kΩ
	DC Operating Voltage	No Input Signal	2.3	2.8	3.3	V
SSC INPUT (Pin 4)						
	Burst Gate Threshold		7.0	7.5	8.0	V
	Line Blanking Threshold		3.1	3.4	3.8	V
	Frame Blanking Threshold / Fast Blanking		0.5	1	1.5	V
	Input Current				60	µA
CONTRAST CONTROL INPUT (Pin 5) (See Figure 1)						
	Input Current				10	µA
	Contrast Control Range		20			dB
SATURATION CONTROL INPUT (Pin 9) (See Figure 2)						
	Input Current				10	µA
	Tracking between Luminance and Chrominance Signals over 10 dB Contrast Control				2	dB
BRIGHTNESS CONTROL INPUT (Pin 1) (See Figure 3)						
	Input Current				10	µA
ACC CAPACITOR (Pin 12)						
	Charging Current	During Burst Gate Period		100		µA
	Discharging Current	During Burst Gate Period			10	µA
	Leakage Current	Out of Burst Gate Period			5	µA
KILLER CAPACITOR (Pin 13)						
	Color off Voltage	No Chroma Signal		5.6		V
	Color on Voltage			6		V
	PAL flip-flop inhibition level			3.2		V
	Control Current			150		µA
	Leakage Current				5	µA
	Voltage with Nominal Input Signal		6.4	6.5	7.0	V
PLL LOOP FILTER (Pin 16)						
	Control Current			800		µA
	Leakage Current				5	µA
SUBCARRIER OUTPUT (Pin 8)						
	Output Burst Amplitude	Within ACC Control Range	1.6	2.4	3.0	V$_{PP}$

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

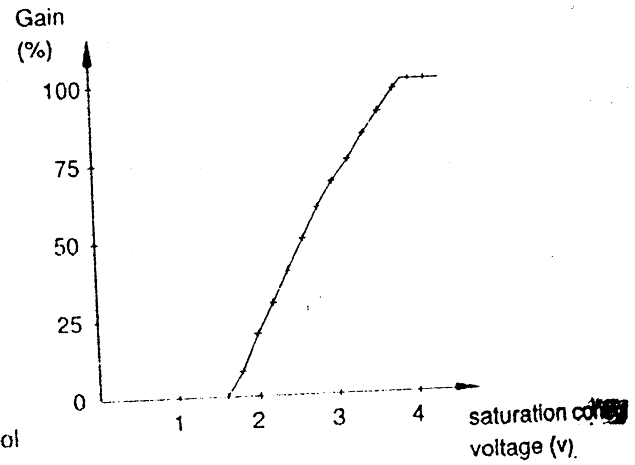
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DELAYED CHANNEL INPUT (Pin 6)						
	DC Operating Voltage	No Input Signal	2.0	2.2	2.4	V
	Input impedance		6	8	12	kΩ
RGB OUTPUTS (Pins 17-18-19)						
	Output Signal Amplitude (Black to White)	• 0.35V B to W. Signal @ Pin 3 • Contrast @ 4.2V • Sat. @ 1.6V • Brig. @ 3.5V	2.80	3.15	3.50	V
	Blue Channel Output Amplitude (no Y)	• 300 mV$_{PP}$ (B-Y), Signal with 200mV$_{PP}$ Burst Amplitude at pin 10 • Contrast @ 4.2V • Sat. @ 4.2V • Brig. @ 3.5V	3.5	3.9	4.3	V$_{PP}$
	Individual Output Sinking Current				2	mA
RGB OUTPUTS (Pins 17-18-19)						
	Maximum Peak White Level		7.8	8.1	8.4	V
	Blanking Level		1.0	1.2	1.4	V
	Black Level Differential Error				300	mV
	Relative Variation in Black Level with Various Saturation, Contrast and Brightness Control Level				10	mV
	Black Level Thermal Drift			0.5		mV/°C
	Differential Black Level Drift over 40°C Temperature Range			5		mV
	Frequency Response(-3dB)			5		MHz
XTAL (Pin 14)						
	Catching Range		± 500	± 700		Hz
RGB CLAMP CAPACITOR (Pin 2)						
	Control Current		50	100	150	µA
	Leakage Current				5	µA

Figure 1 : Contrast Control Voltage Range.



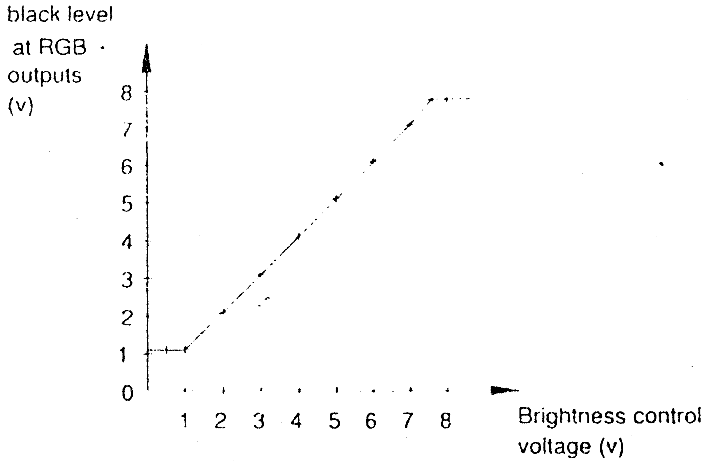
91DSTDA8217-03

Figure 2 : Saturation Control Voltage Range.



91DSTDA8217-04

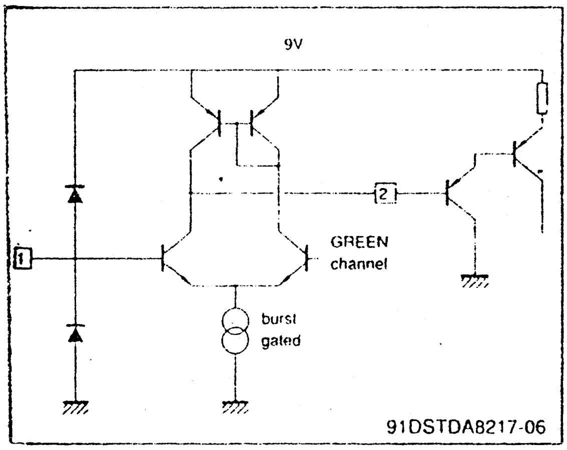
Figure 3 : Brightness Control Voltage Range.



91DSTDA8217-05

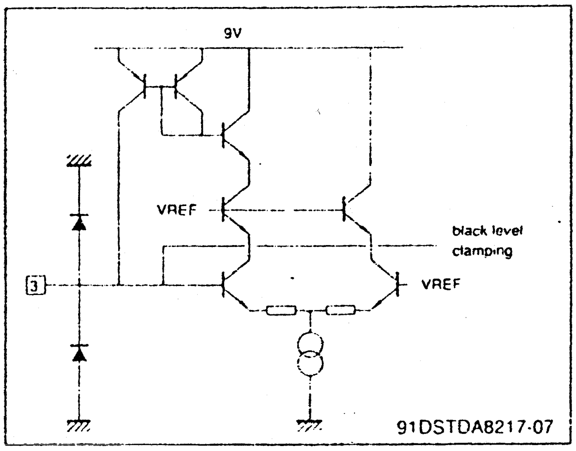
INPUT / OUTPUT PIN CONFIGURATION

Figure 4 : Pins 1 - 2 Configuration.


9V
1
2
GREEN channel
burst gated

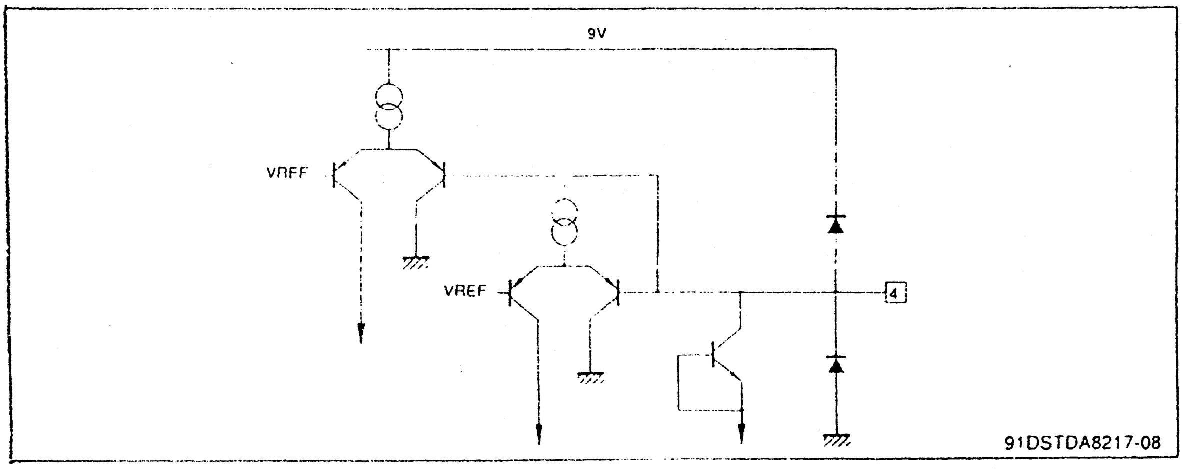
91DSTDA8217-06

Figure 5 : Pin 3 Configuration.


9V
VREF
black level clamping
3
VREF

91DSTDA8217-07

Figure 6 : Pin 4 Configuration.


9V
VREF
VREF
4

91DSTDA8217-08

INPUT / OUTPUT PIN CONFIGURATION (continued)

Figure 7 : Pin 5 Configuration.

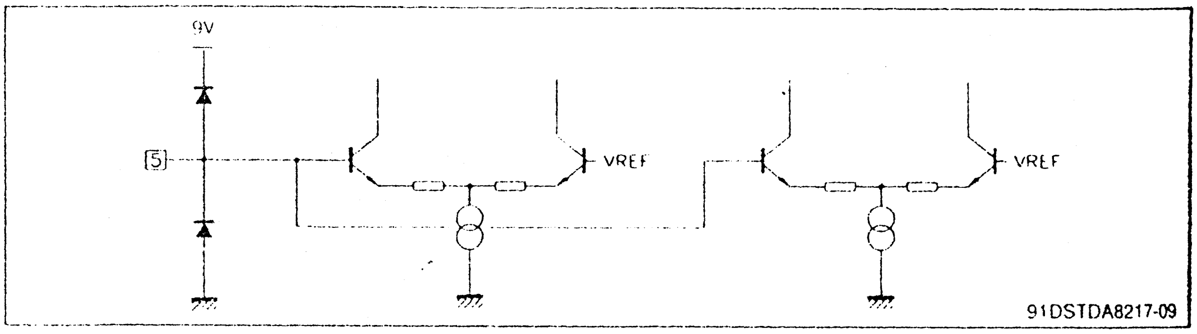

9V
5
VREF
VREF
91DSTDA8217-09

Figure 8 : Pin 6 Configuration.

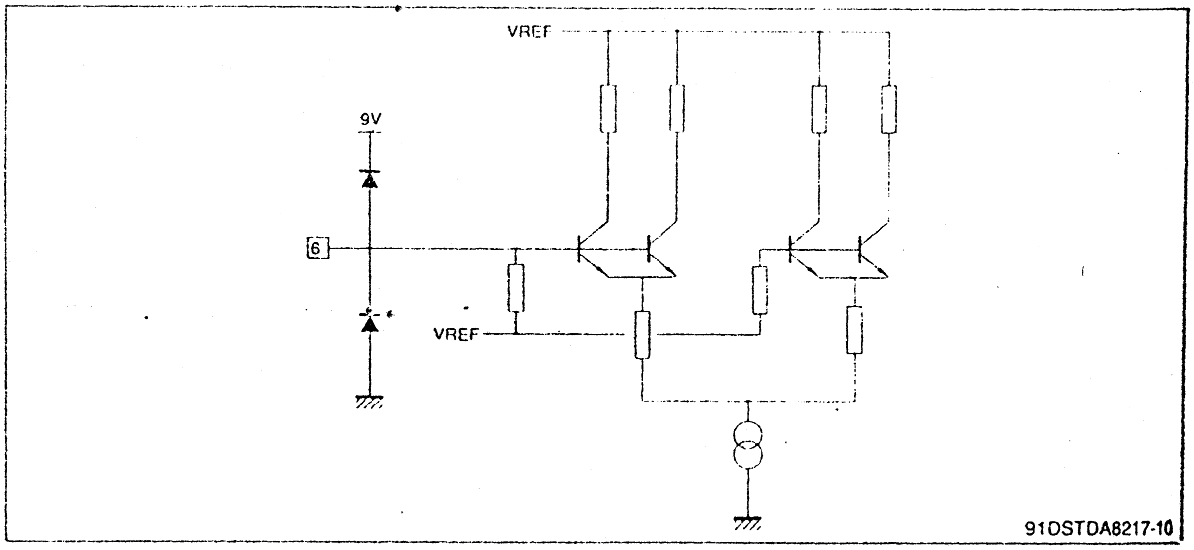

VREF
9V
6
VREF
91DSTDA8217-10

Figure 9 : Pin 8 Configuration.

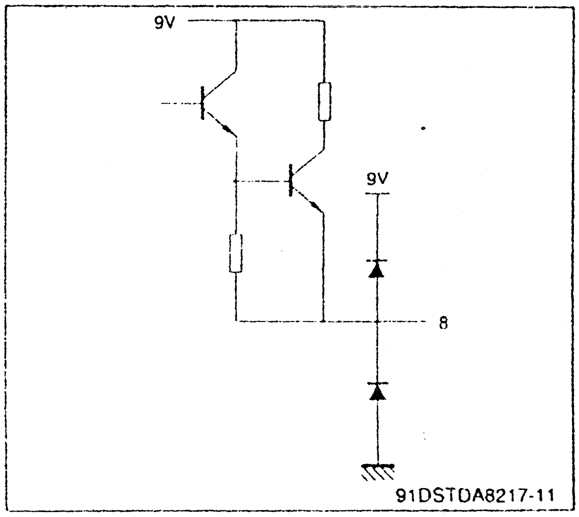
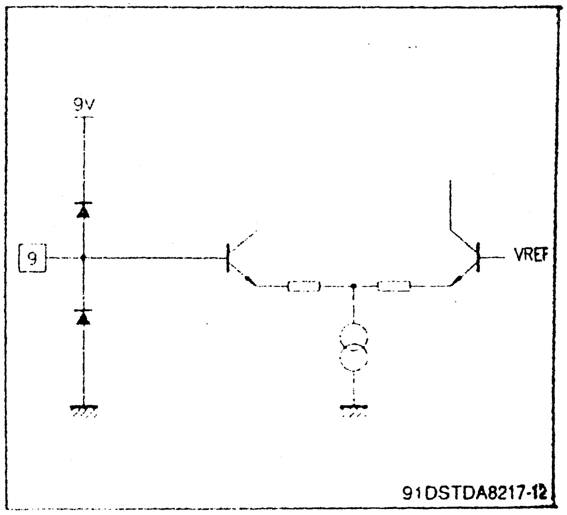

9V
9V
8
91DSTDA8217-11

Figure 10 : Pin 9 Configuration.


9V
9
VREF
91DSTDA8217-12

INPUT / OUTPUT PIN CONFIGURATION (continued)

Figure 11 : Pin 10 Configuration.

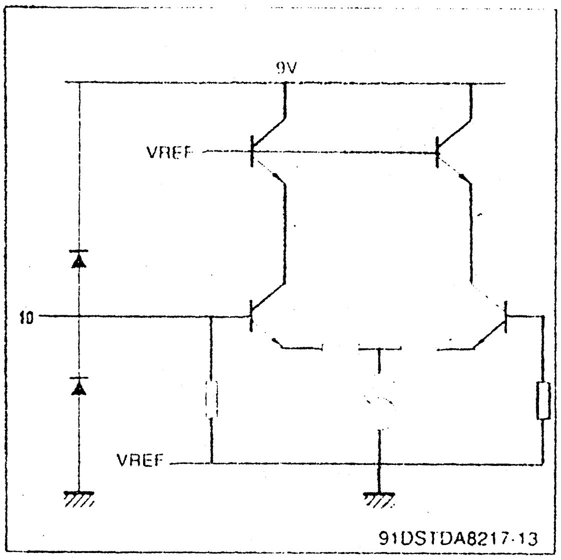

9V
VREF
10
VREF
91DSTDA8217-13

Figure 12 : Pin 12 Configuration.

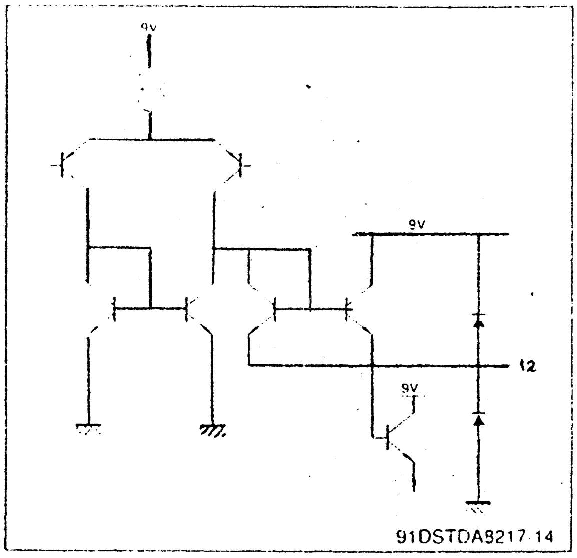

9V
9V
12
9V
91DSTDA8217-14

Figure 13 : Pin 13 Configuration.

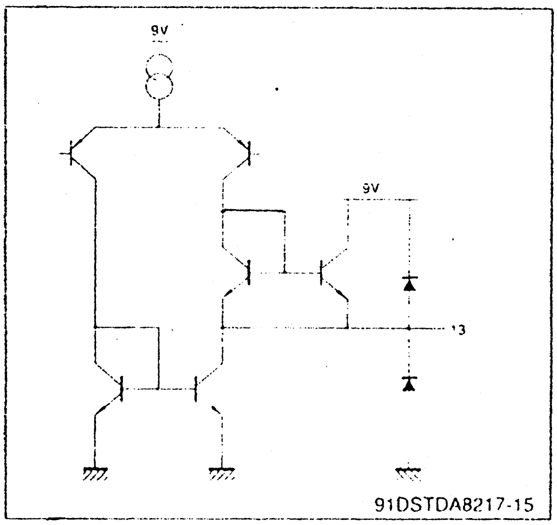

9V
9V
13
91DSTDA8217-15

Figure 14 : Pin 14 Configuration.

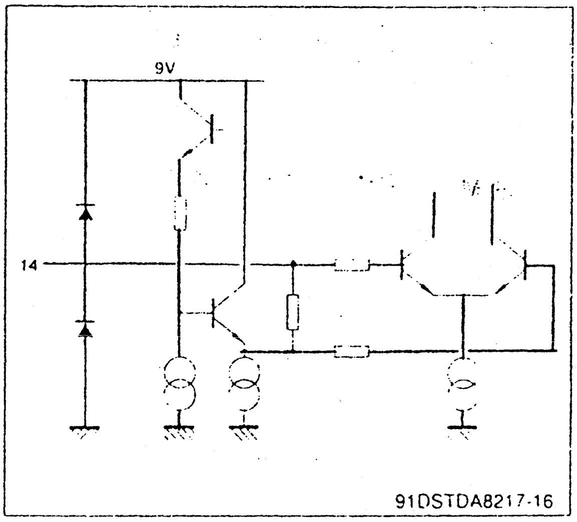

9V
14
91DSTDA8217-16

Figure 15 : Pin 16 Configuration.

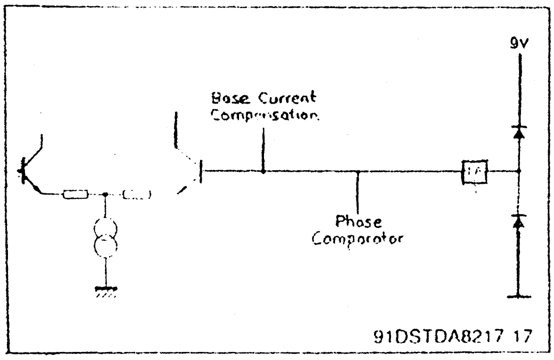
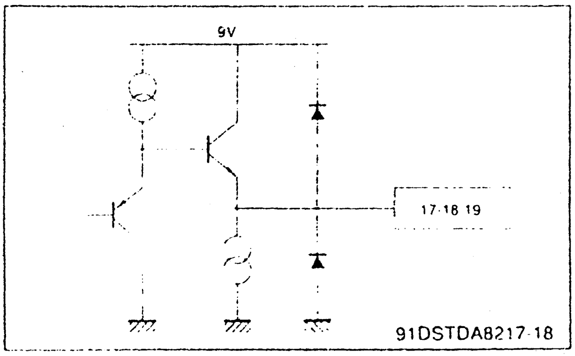
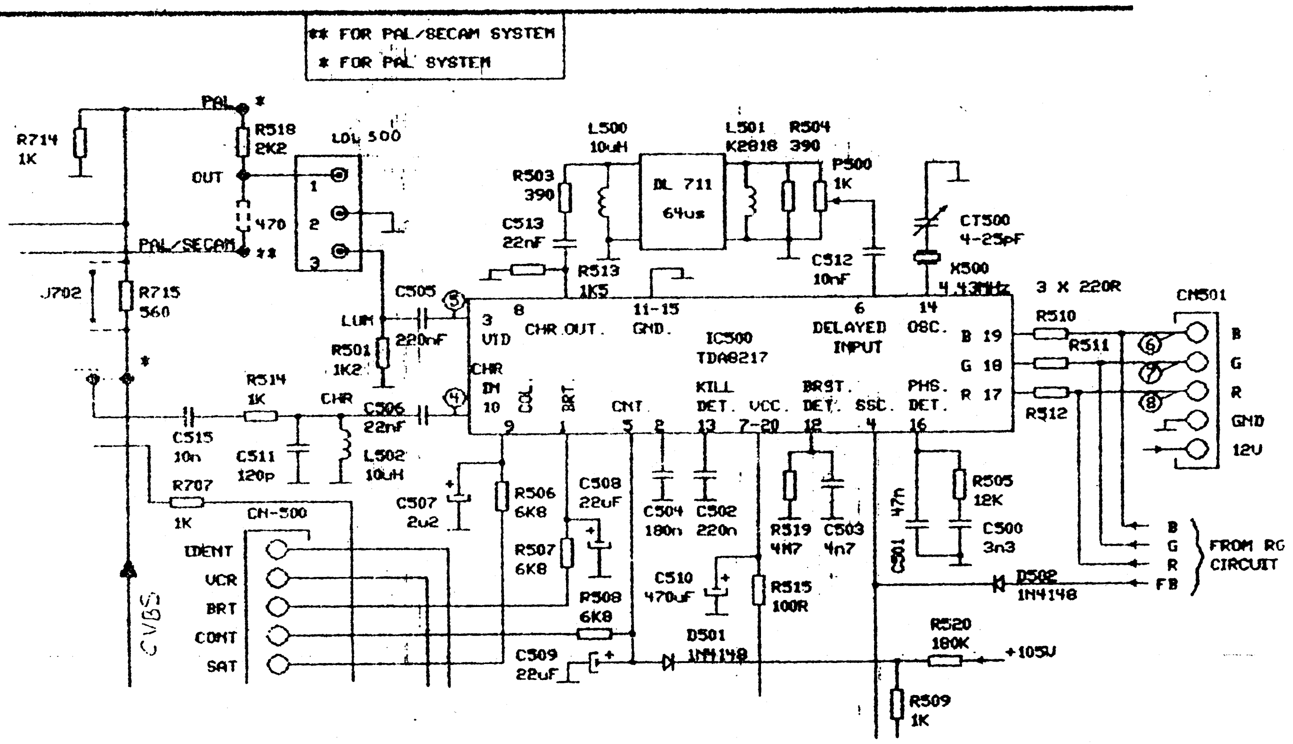

9V
Base Current Compensation
Phase Comparator
91DSTDA8217 17

Figure 16 : Pins 17 - 18 - 19 Configuration.

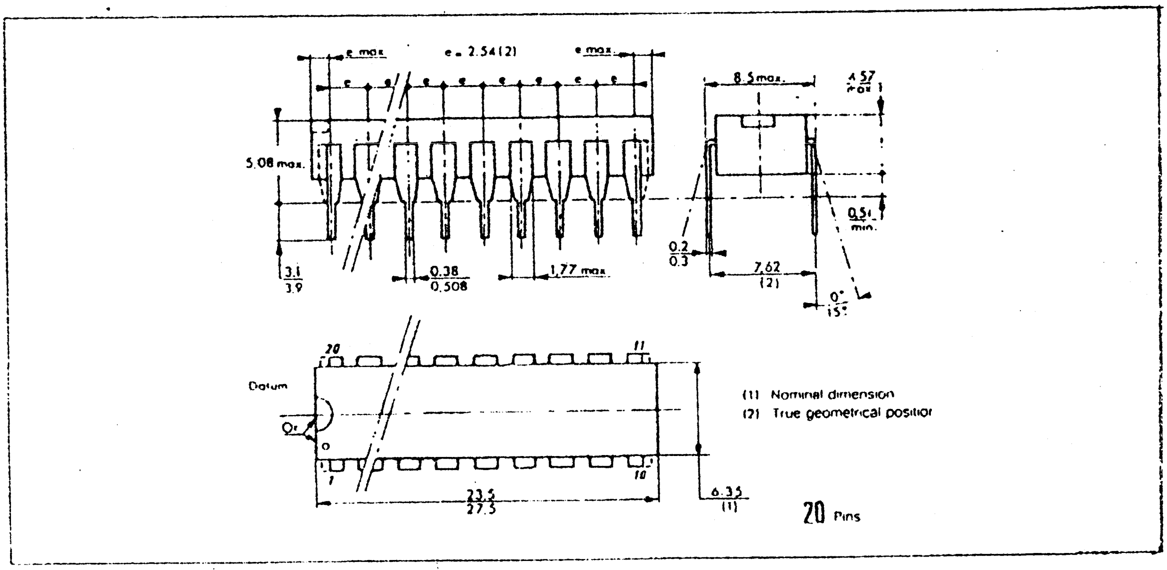

9V
17-18 19
91DSTDA8217-18

TDA8217

APPLICATION DIAGRAM (with OSD capability)


** FOR PAL/SECAM SYSTEM
* FOR PAL SYSTEM
PAL
PAL/SECAM
OUT
R714 1K
R518 2K2
470
J702
R715 560
LDL 500
LUM
R501 1K2
C505 220nF
CHR
C506 22nF
R514 1K
C515 10n
C511 120p
L502 10uH
R707 1K
CN-500
IDENT
VCR
BRT
CONT
SAT
CVBS
L500 10uH
R503 390
C513 22nF
DL 711 64us
R513 1K5
L501 K2818
R504 390
P500 1K
C512 10nF
CT500 4-25pF
X500 4.43MHz
3 VID
8 CHR.OUT.
11-15 GND.
IC500 TDA8217
6 DELAYED INPUT
14 OSC.
CHR IN 10
COL. 9
BRT. 1
CNT. 5
2
KILL DET. 13
VCC. 7-20
BRST. DET. 12
SSC. 4
PHS. DET. 16
B 19
G 18
R 17
3 X 220R
R510
R511
R512
CN501
B
G
R
GND
12V
C507 2u2
R506 6K8
R507 6K8
C508 22uF
R508 6K8
C509 22uF
C504 180n
C502 220n
C510 470uF
D501 1N4148
R519 4M7
C503 4n7
R515 100R
C501 47n
R505 12K
C500 3n3
D502 1N4148
R520 180K
+105V
R509 1K
FB
FROM RG CIRCUIT

PACKAGE MECHANICAL DATA : 20 Pins - Plastic DIP

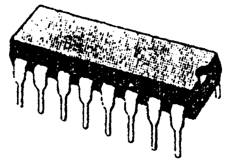

e max
e = 2.54 (2)
e max
5.08 max
3.1
3.9
0.38
0.508
1.77 max
8.5 max
4.57 max
0.51 min
0.2
0.3
7.62 (2)
0°
15°
20
11
Datum
1
10
23.5
27.5
6.35 (1)
(1) Nominal dimension
(2) True geometrical position
20 Pins

RGB SWITCHING CIRCUIT

TEA5114A

RGB SWITCHING CIRCUIT

- 25 MHz BANDWIDTH
- CROSSTALK : 55 dB
- SHORT CIRCUIT TO GROUND OR V_{CC} PROTECTED
- ANTI SATURATION GAIN CHANGING
- VIDEO SWITCHING



DIP16
(Plastic package)

ORDER CODE : TEA5114A

DESCRIPTION

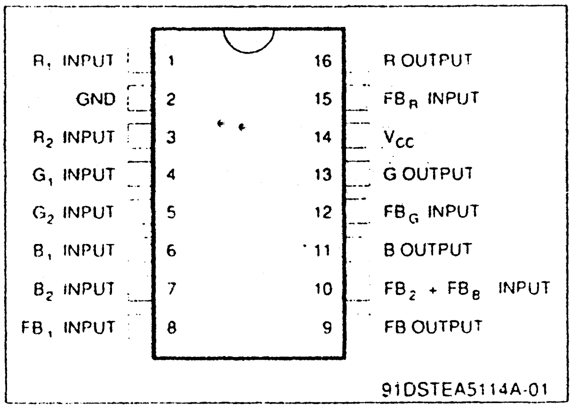
This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set.

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

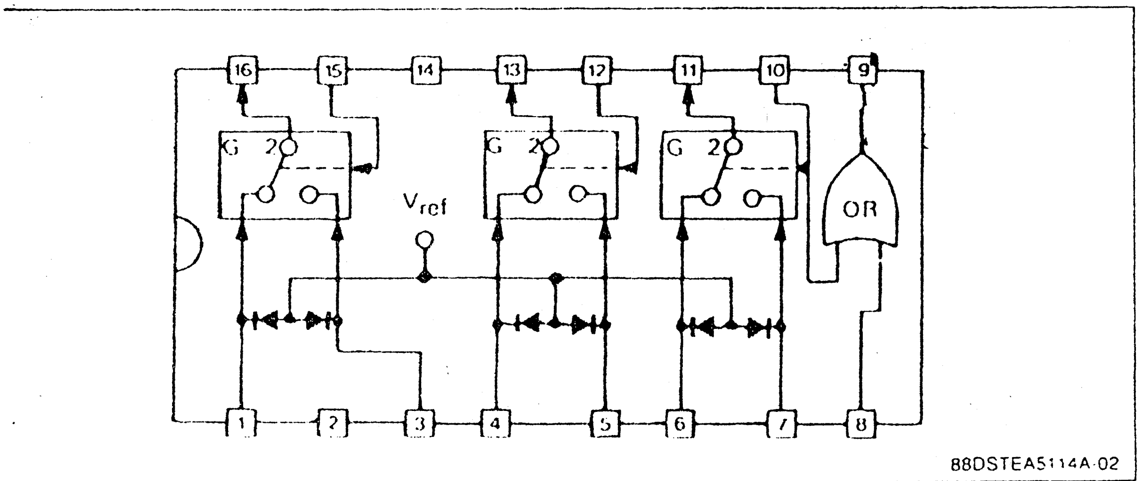
An AC output signal higher than 2 Vpp makes gain going slowly down to 0 dB to protect the TV set video amplifier from saturation.

Fast blanking output is a logicial OR between FB1 (Pin 8) and FB2 (Pin 10).

PIN CONNECTIONS


R1 INPUT 1
GND 2
R2 INPUT 3
G1 INPUT 4
G2 INPUT 5
B1 INPUT 6
B2 INPUT 7
FB1 INPUT 8
16 R OUTPUT
15 FBR INPUT
14 VCC
13 G OUTPUT
12 FBG INPUT
11 B OUTPUT
10 FB2 + FBB INPUT
9 FB OUTPUT
91DSTEA5114A-01

BLOCK DIAGRAM


16
15
14
13
12
11
10
9
G 2
G 2
G 2
Vref
OR
1
2
3
4
5
6
7
8
88DSTEA5114A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		18	V
T_j	Junction Temperature		– 40 to 150	°C
T_{stg}	Storage Temperature		– 40 to 150	°C
Z_l	Minimum Load Resistor on Each Output	V_{CC} = 12 V V_{CC} = 10 V	300 150	Ω Ω
T_{amb}	Operating Ambient Temperature		0 to 70	°C

THERMAL DATA

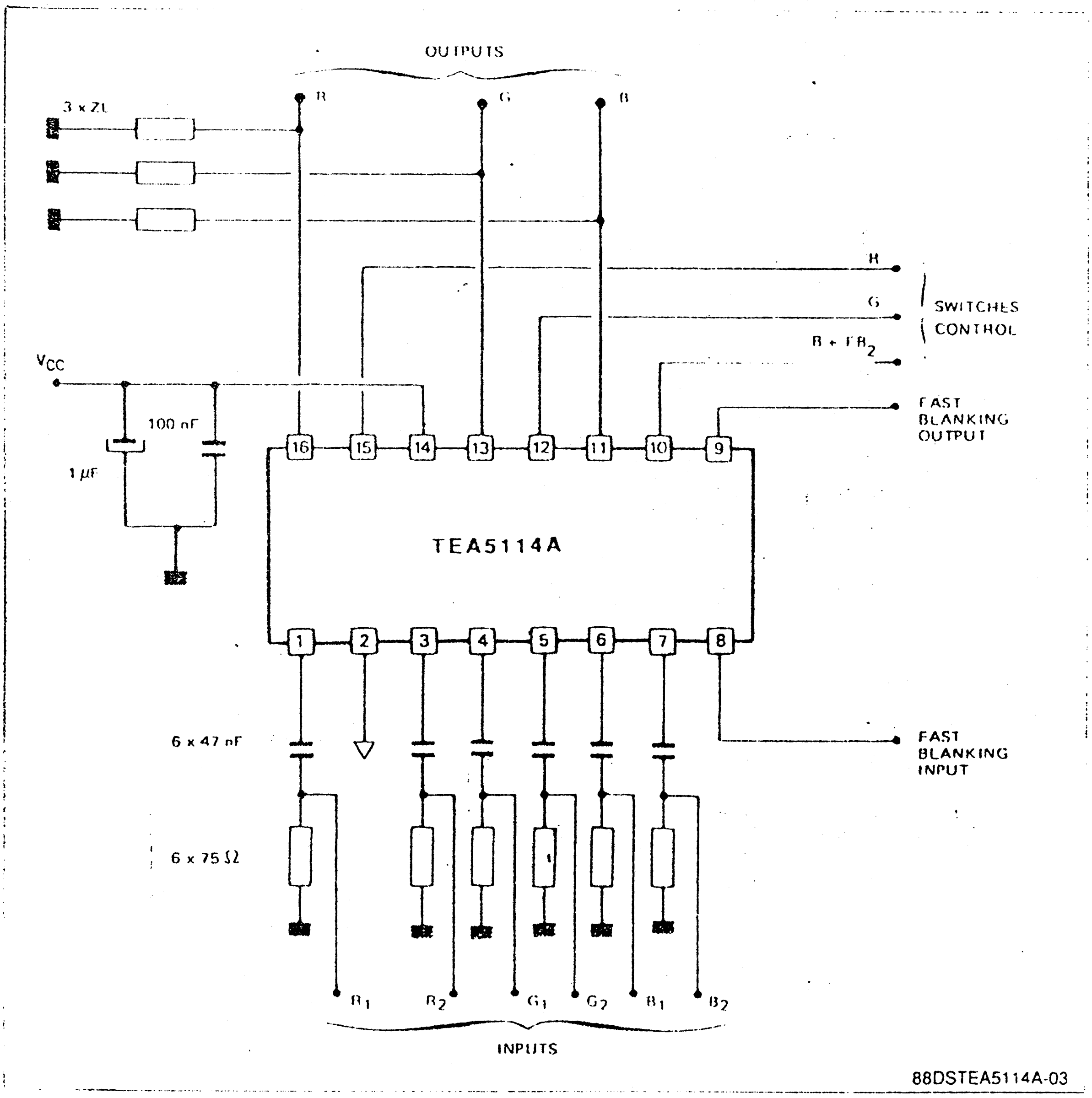
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 12 V, Z_L (RGB) = 300 Ω
V_{CC} = 10 V, Z_L (RGB) = 150 Ω (unless otherwise specified)

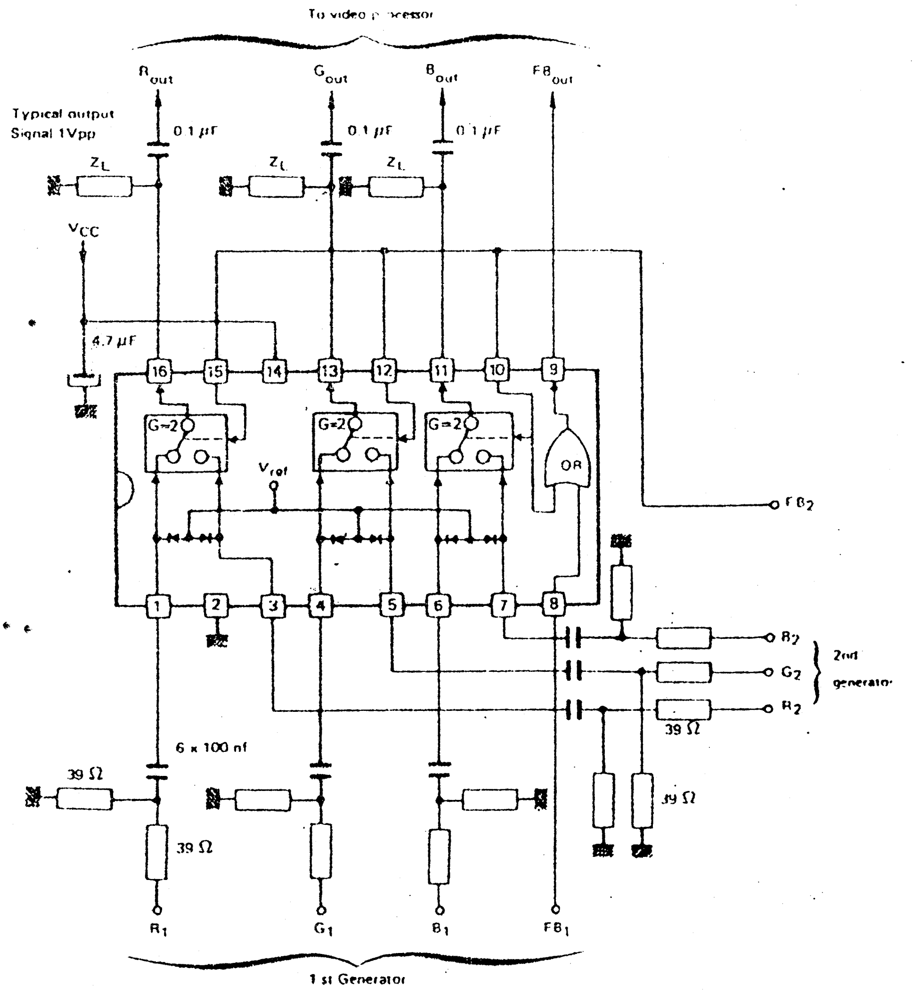
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	9	12	13.2	V
I_{CC}	Supply Current without Load V_{CC} = 12 V	20	30	40	mA
V_{ON}	Black Level Output Voltage (on pins 11, 13, 16 square wave output signal 1 kHz - 1 Vpp) T_j = 25 °C (5mV/°C typical variation)	1.8	2.5	2.9	V
G_{RGB}	Gain of Each Channel Pins 11, 13, 16 F = 1 MHz , V_{in} = 0.5 V_{pp}	5	5.5	6	dB
B_{RGB}	Bandwidth (– 3 dB) V_O = 1 V_{pp}	18	22		MH
V_{GC}	Threshold Output Voltage for Gain Changing (– 0.5 dB)	2			V
V_R	Video Rejection between Two Inputs R, G or B F = 1 MHz Sinus V_O = 1 V_{pp}	50	55		dB
Z_{IRGB}	Input Impedance on Pins 1, 3, 4, 5, 6, 7 V_O = 1 V_{pp}	10			KΩ
Z_{ORGB}	R, G, B Output Impedance on Pins 11, 13, 16			15	Ω
T_{FB}	FB rising and falling time on pin 9. 1 Vpp Input Voltage Pins 8, 10		20		[illegible]
V_{IHFB}	FB High Level Input Voltage on Pins 8, 10, 12, 15	1		4	[illegible]
V_{ILFB}	FB Low Level Input Voltage on Pins 8, 10, 12, 15	0		0.4	[illegible]
Z_{IFB}	Input Impedance on Pins 8, 10, 12, 15	0.7	1	1.3	K
V_{OHFB}	High Level FB Output Voltage (pin 9) Input 1 V on Pins 8, 10	0.8	1	1.2	[illegible]
V_{OLFB}	Low Level FB Output (pin 9) Input 0 V on Pins 8, 10			0.3	[illegible]
Z_{OFB}	FB Output Impedance Pin 9 High Level			30	[illegible]
T_{dFBRGB}	Delay Time between FB Inputs and R, G, B Switching		20		[illegible]

TEST DIAGRAM


OUTPUTS
R
G
B
3 x ZL
R
G
B + FB2
SWITCHES CONTROL
VCC
100 nF
1 µF
FAST BLANKING OUTPUT
16
15
14
13
12
11
10
9
TEA5114A
1
2
3
4
5
6
7
8
6 x 47 nF
FAST BLANKING INPUT
6 x 75 Ω
R1
R2
G1
G2
B1
B2
INPUTS
88DSTEA5114A-03

TYPICAL R, G, B SWITCHING APPLICATION

Vcc = 12 V   Zₗ ≥ 300 Ω.
Vcc = 10 V   Zₗ ≥ 150 Ω.

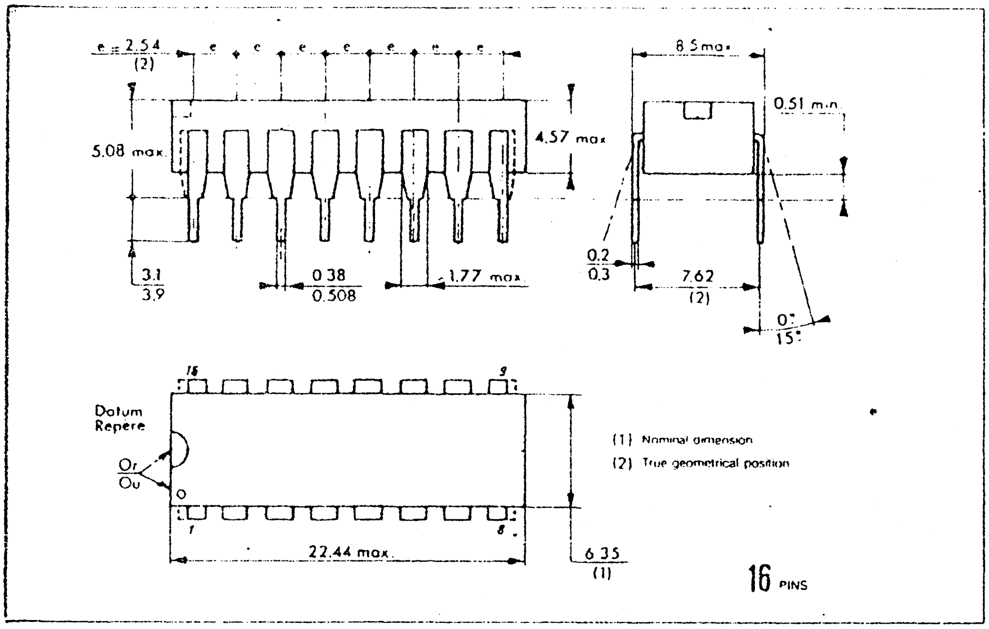

To video processor
Rout
Gout
Bout
FBout
Typical output
Signal 1Vpp
0.1 µF
0.1 µF
0.1 µF
ZL
ZL
ZL
VCC
4.7 µF
16
15
14
13
12
11
10
9
G=2
G=2
G=2
OR
Vref
FB2
1
2
3
4
5
6
7
8
B2
G2
R2
2nd
generator
39 Ω
6 x 100 nf
39 Ω
39 Ω
39 Ω
R1
G1
B1
FB1
1 st Generator

Peritelevision plug standard input value 1 Vpp.

88DSTEA5114A-01

PACKAGE MECHANICAL DATA

16 Pins – Plastic DIP

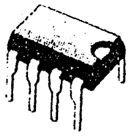

e = 2.54
(2)
e
5.08 max.
4.57 max
3.1
3.9
0.38
0.508
1.77 max.
8.5 max
0.51 min
0.2
0.3
7.62
(2)
0°
15°
16
9
Datum
Repere
Or
Ou
1
8
22.44 max.
6.35
(1)
(1) Nominal dimension
(2) True geometrical position
16 PINS

VIDEO SWITCH

TEA2014A

VIDEO SWITCH

- 1 VIDEO OUTPUT 75 Ω - 1 V_{PP} NOT SWITCHED
- 1 SWITCHED VIDEO OUTPUT 2 V_{PP}
- VIDEO CROSSTALK : 50 dB TYPICAL
- SHORT CIRCUIT PROTECTION OF INPUTS AND OUTPUTS
- CLAMPED VIDEO INPUTS



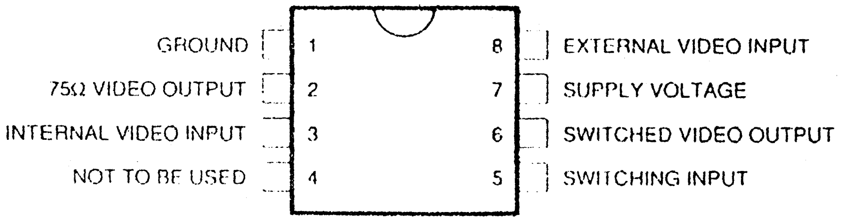
DIP8
(Plastic package)

ORDER CODE : TEA2014A

DESCRIPTION

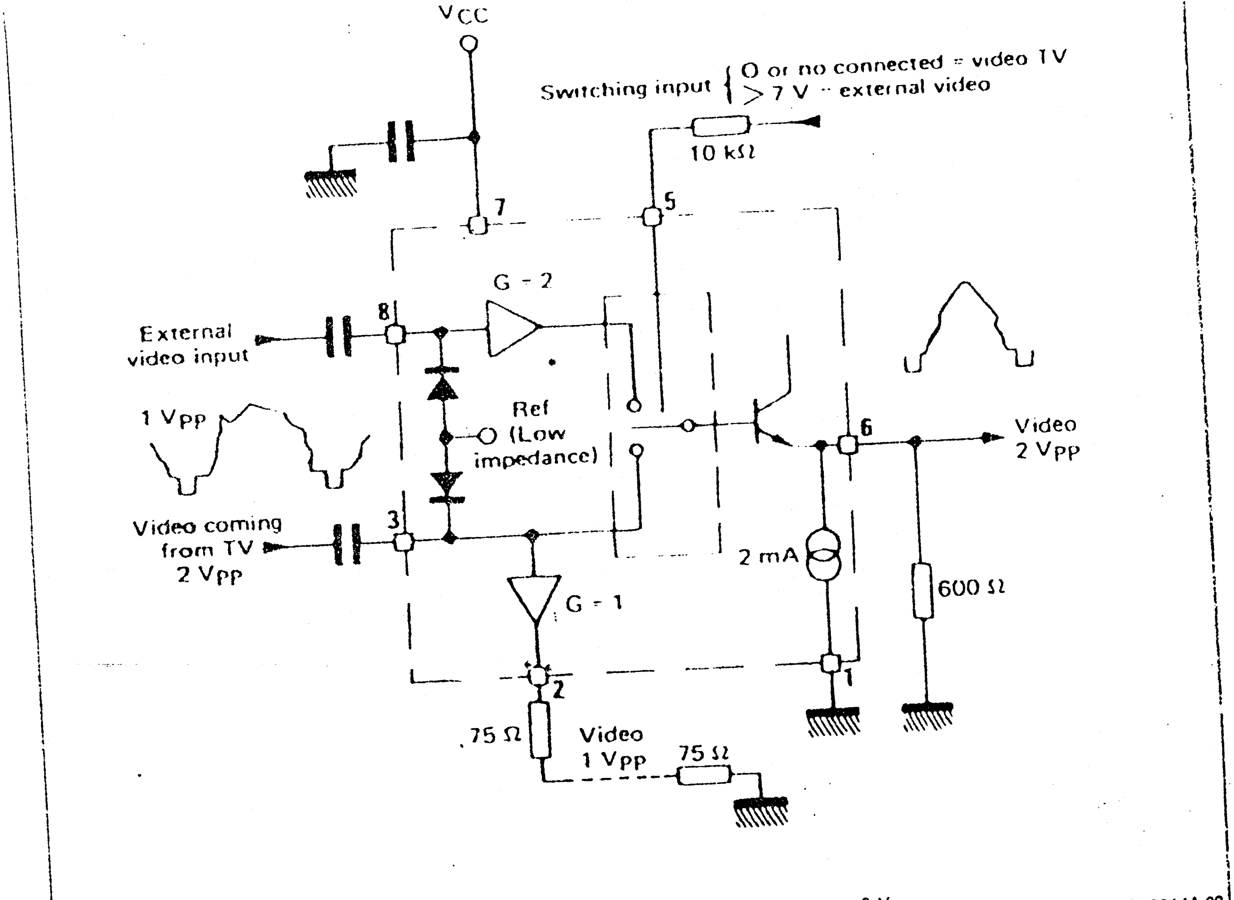
This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set. The TEA2014A is supplied in a DIL8.

PIN CONNECTIONS


GROUND
75Ω VIDEO OUTPUT
INTERNAL VIDEO INPUT
NOT TO BE USED
1
2
3
4
8
7
6
5
EXTERNAL VIDEO INPUT
SUPPLY VOLTAGE
SWITCHED VIDEO OUTPUT
SWITCHING INPUT

91DSTEA2014A-01

TYPICAL APPLICATION AND TEST CIRCUIT


VCC
Switching input { O or no connected = video TV
> 7 V = external video
10 kΩ
7
5
G = 2
8
External video input
1 Vpp
Ref (Low impedance)
Video coming from TV 2 Vpp
3
G = 1
2 mA
6
Video 2 Vpp
600 Ω
1
2
75 Ω
Video 1 Vpp
75 Ω

We advice to protect the 75 Ω output through a 75 Ω resistor for supply voltage higher than 9 V

88DSTEA2014A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{oper}	Operating Temperature with Load > 150 Ω on PIN 2 with Load = 75 Ω on PIN 2	 0, + 100 0, + 70	°C
T_j	Junction Temperature	– 40, + 150	°C
T_{stg}	Storage Temperature	– 40, + 150	°C
–	Minimum DC Load Resistor PIN 6 Minimum DC Load Resistor PIN 2	600 75	Ω Ω

THERMAL DATA

$R_{th (j-a)}$	Junction-ambient Thermal Resistance	90 Typ	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C V_{CC} = 9 V (unless otherwise specified

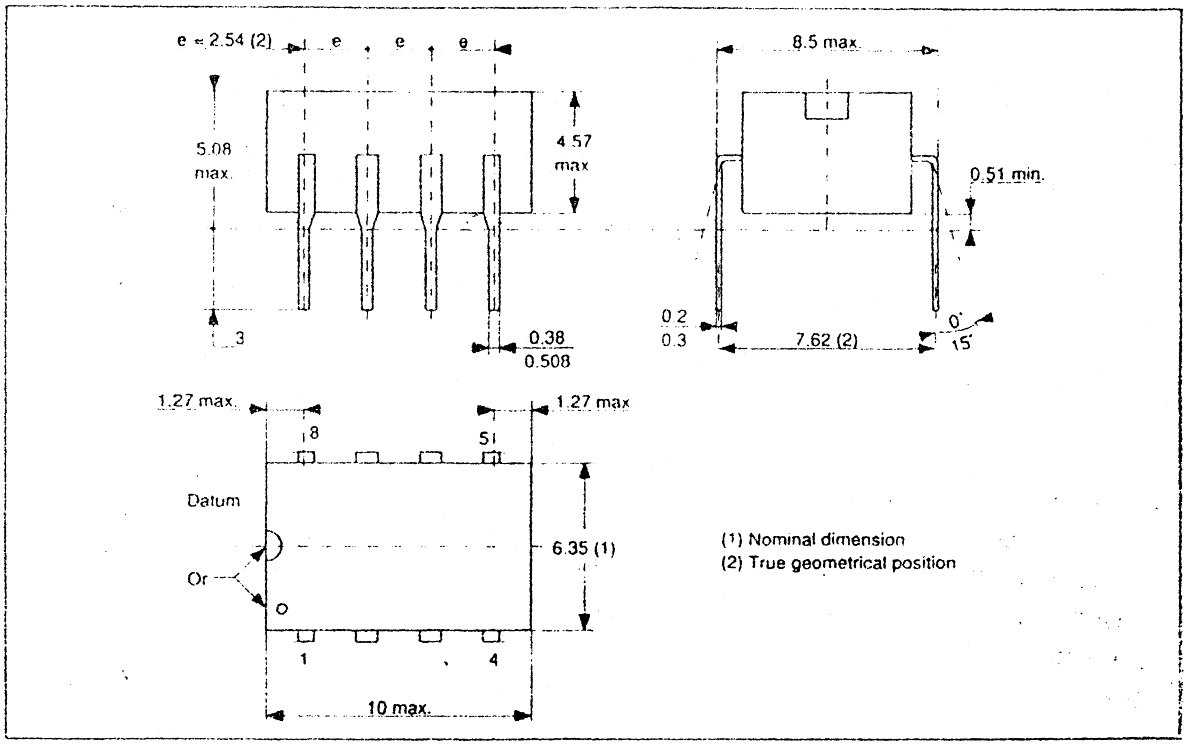
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage Range	8	-	14	V
I_{CC}	Supply Current (no load on pin 2 and pin 6)	–	–	20	mA
I_{CC}	Supply Current (with 75 Ω pin 2 1, with 600 Ω between pin 6 1)	-	45	-	mA
P_{tot}	Total Power Dissipation with Load	-	400	-	mW
INPUTS (pin 8 and pin 3)					
–	Internal Video Input Swing from Picture IF (positive Video)	–	–	4.5	Vpp
–	Internal Video Input Impedance (positive video)	50	–	–	kΩ
–	Internal Video Input Bias Current (positive video)	6	25	40	µA
–	External Video Input Swing (positive video)	-	-	2	Vpp
–	External Video Input Impedance (positive video)	50	–	-	kΩ
SWITCHED OUTPUT (pin 6) - R_{LOAD} = 600 Ω					
–	Video Output Swing	4	–	–	Vpp
–	Video Output Dynamic Impedance	–	–	25	Ω
–	Video DC Output Voltage (sync. pulse level note 1)	1.7	2	2.4	V
–	Video Bandwith Pin 6 – from Internal Input pin 3 (– 1 dB)	6	–	–	MHz
–	Video Bandwith Pin 6 – from External Input Pin 8 (– 3 dB)	6	–	–	MHz
–	Output Gain Pin 6 – Pin 8	+ 5	+ 6	+ 7	dB
–	Output Gain Pin 6 – Pin 3	– 1	– 0.5	0	dB
EXTERNAL OUTPUT (pin 2) - R_{LOAD} = 75 Ω					
–	Video Output Swing	2.2	–	–	Vpp
–	Video Output Dynamic Impedance	–	10	–	Ω
–	Video DC Output Voltage (sync. pulse level . note 1)	1.7	2	2.4	V
–	Video Bandwidth (– 1dB)	6	–	–	MHz
–	Video Output Gain (pin 2 – pin 3)	– 1.8	– 1	– 0.4	dB
SWITCHING INPUT (pin 5)					
–	Switching Input Unactive Low Level or Unconnected Pin (TV receiving)	0	–	3	V
–	Switching Input Active Level (ext. receiving)	7	–	Vcc	V
–	Switching Input Impedance	10	–	–	kΩ
OTHER DYNAMIC FEATURES					
–	Video rejection Between Two Inputs 1MHz 1kHz	 – – 50	 – 50 –	 – –	 dB dB
–	Linearity Distortion Luma (test line 17) Chroma (test line 331) Intermodulation Luma – Chroma (test line 331)	 – – –	 2 2 5	 – – –	 % % %
–	Supply Voltage Rejection (1 kHz)	40	50	–	dB

TAB-03

Note : 1. Use a video signal with a synchro pulse in order to make the clamp work in a correct way (75 Ω to the ground and 10 µF in series)

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP


e = 2.54 (2)
e
e
e
5.08
max.
4.57
max
3
0.38
0.508
8.5 max.
0.51 min.
0.2
0.3
7.62 (2)
0°
15°
1.27 max.
1.27 max
8
5
Datum
Or
6.35 (1)
1
4
10 max.
(1) Nominal dimension
(2) True geometrical position

TUNING CIRCUIT

TUNING SECTION

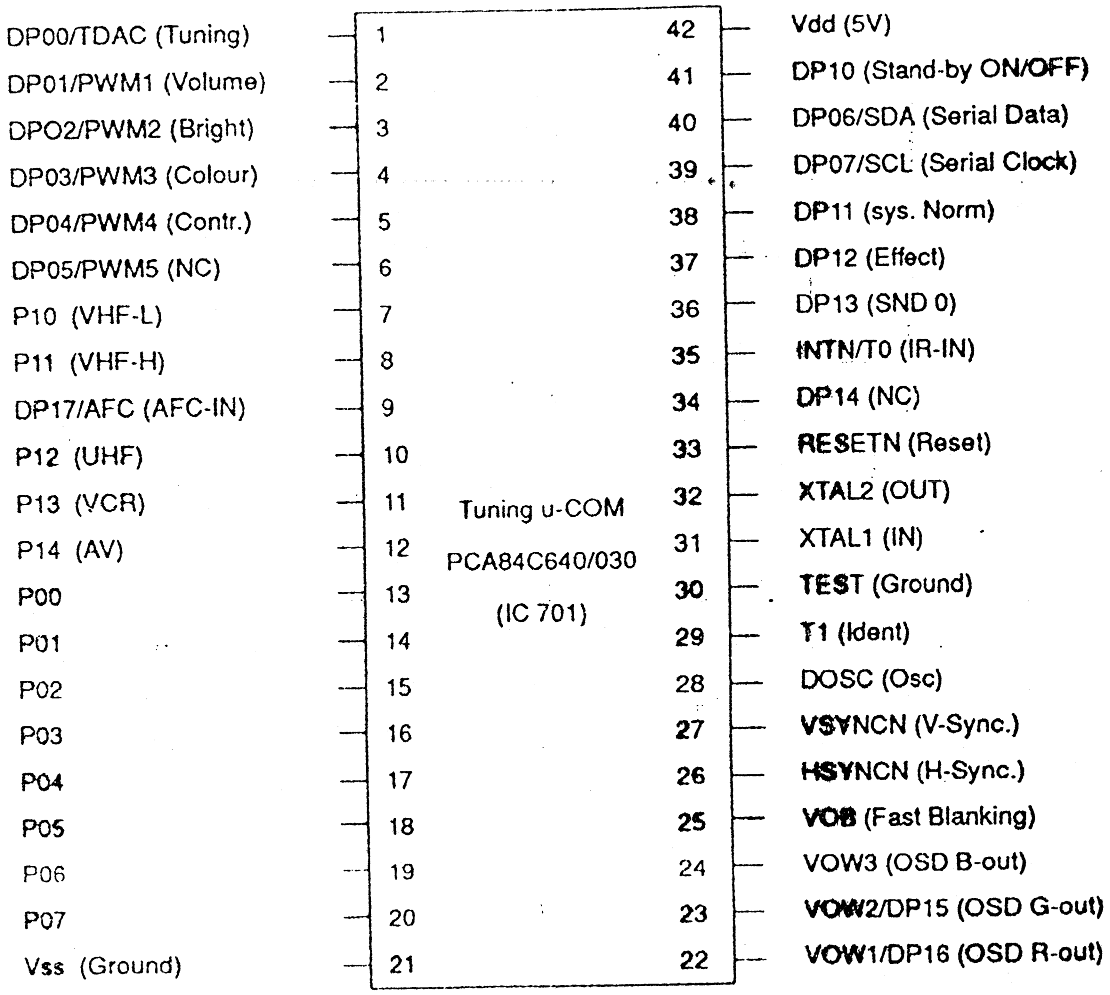
1. Summary:

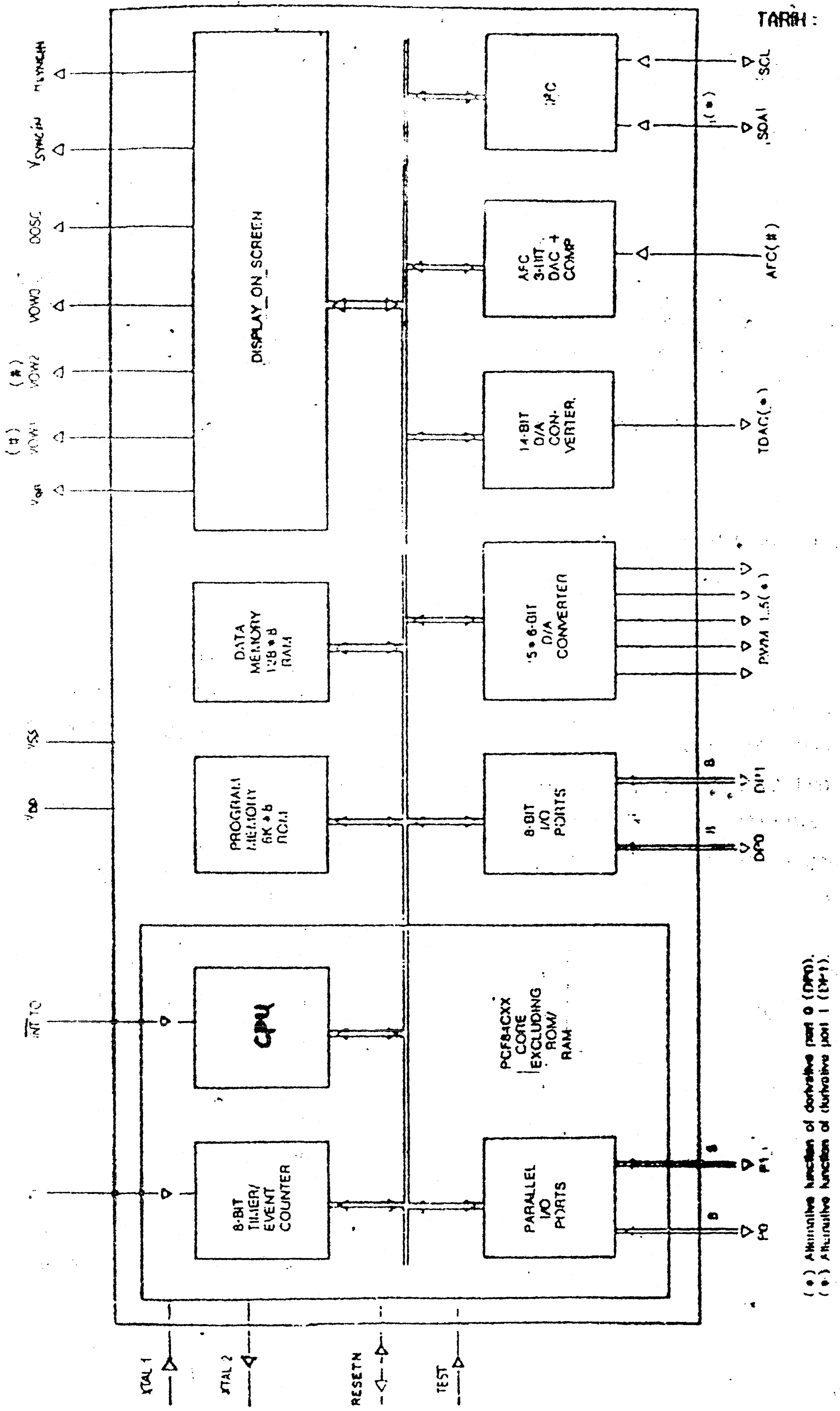
The name of microcontroller for this tuning section is PCA84C640/030 which is CMOS and includes the PCA84C processor core, 6144 bytes mask programmable program ROM, 128 bytes RAM, a multimaster I²C - bus interface, 1 external interrupt line, 1 direct testable line, 18 general purpose bi-directional I/O lines + 11 function combined I/O lines, one 14-bit PWM analog control and an AFC input (3 bit DAC + comparator) for Voltage Synthesized Tuning, five 6-bit PWM analog control outputs and a Display On Screen facillity for two lines of 16 characters (max. 48 character types, 8 X 9 dot font).

2. Block diagram (PCA84C640/030)

Refer to Fig. 1.2

3. Pinning Diagram


DP00/TDAC (Tuning) 1
DP01/PWM1 (Volume) 2
DPO2/PWM2 (Bright) 3
DP03/PWM3 (Colour) 4
DP04/PWM4 (Contr.) 5
DP05/PWM5 (NC) 6
P10 (VHF-L) 7
P11 (VHF-H) 8
DP17/AFC (AFC-IN) 9
P12 (UHF) 10
P13 (VCR) 11
P14 (AV) 12
P00 13
P01 14
P02 15
P03 16
P04 17
P05 18
P06 19
P07 20
Vss (Ground) 21
42 Vdd (5V)
41 DP10 (Stand-by ON/OFF)
40 DP06/SDA (Serial Data)
39 DP07/SCL (Serial Clock)
38 DP11 (sys. Norm)
37 DP12 (Effect)
36 DP13 (SND 0)
35 INTN/T0 (IR-IN)
34 DP14 (NC)
33 RESETN (Reset)
32 XTAL2 (OUT)
31 XTAL1 (IN)
30 TEST (Ground)
29 T1 (Ident)
28 DOSC (Osc)
27 VSYNCN (V-Sync.)
26 HSYNCN (H-Sync.)
25 VOB (Fast Blanking)
24 VOW3 (OSD B-out)
23 VOW2/DP15 (OSD G-out)
22 VOW1/DP16 (OSD R-out)
Tuning u-COM
PCA84C640/030
(IC 701)


HSYNCin
VSYNCin
OOSC
VOW3
(★) VOW2
(#) VOW1
VDS
DISPLAY_ON_SCREEN
I²C
SCL
SDA(★)
AFC 3-BIT DAC + COMP
AFC(#)
14-BIT D/A CON-VERTER
TDAC(★)
DATA MEMORY 128 ✱ 8 RAM
5 ✱ 6-BIT D/A CONVERTER
PWM 1..5(★)
VSS
VDD
PROGRAM MEMORY 6K ✱ 8 ROM
8-BIT I/O PORTS
8
DP1
8
DP0
INT T0
CPU
PCF84CXX CORE EXCLUDING ROM/RAM
8-BIT TIMER/ EVENT COUNTER
PARALLEL I/O PORTS
8
P1
8
P0
XTAL 1
XTAL 2
RESETN
TEST
(★) Alternative function of derivative port 0 (DP0).
(#) Alternative function of derivative port 1 (DP1).

(★) Alternative func..on of derivative port 0 (DP0).
(#) Alternative function of derivative port 1 (DP1).

Fig. 1.2 PCA84C640 block diagram

number of terminals.

PIN DESCRIPTTON

Pin number	Pin name	0	Functions
1	DP00/TDAC	1	derivative I/O port or 14 D/A PWM
2..6	DP01-05/PWM1-5	5	derivative I/O port or 6bit D/A PWM
7,8,10..20	P10-P14, P00-P07	13	I/O ports
9	DP17/AFC	1	derivative I/O port or compatator input with 3-bit D/A
40	DP06/SDA	1	derivative open drain I/O port or I²C-bus clock line
39	DP07/SCL	1	derivative open drain I/O port or I²C-bus clock line
35	INTN/TO	1	external interrupt/direct testable
41, 38, 36, 34	DP10-DP14	5	derivative I/O port
23, 22	DP15-16/VOW2-1	2	derivative I/O port or character video output of DOS
33	RESETN	1	initialize input or POR output
32, 31	XTAL2, XTAL1	2	oscillator output/input terminals for system clock
30	TEST	1	control input of test-and emu-mode
29	T1	1	direct testable pin and event counter input
28	DOSC	1	Connection to RC oscillator of DOS clock
27	VSYNCN	1	vertical synchronous signal input
26	HSYNCN	1	horizontal synchronous signal input
25, 24	VOB, VOW3	2	push pull video char. output of DOS
21	VSS	1	Ground terminal
42	VDD	1	power supply terminal

4. Function Description

4-1. RESETN (PIN 33)

This terminal is used as an active low initialize input or as an output of the power on reset circuit. The power on reset circuit monitors the voltage level of Vdd.
If Vdd remains below the internal reference voltage (Vref=1.5 V), the oscillator is inhibit and the reset terminal has an undefined level.
When Vdd rises above Vref, the oscillator starts and reset is pulled down to Vss via TR3 for a period of TD (typ. 50 uS).

Three modes of RESETN are possible:

1. RESETN as a input for an external RESET.

2. VDD rises above the minimum operation voltage before TD is exceeded. Then there are no external components necessary.
(Fig. 2.1. and 2.2).

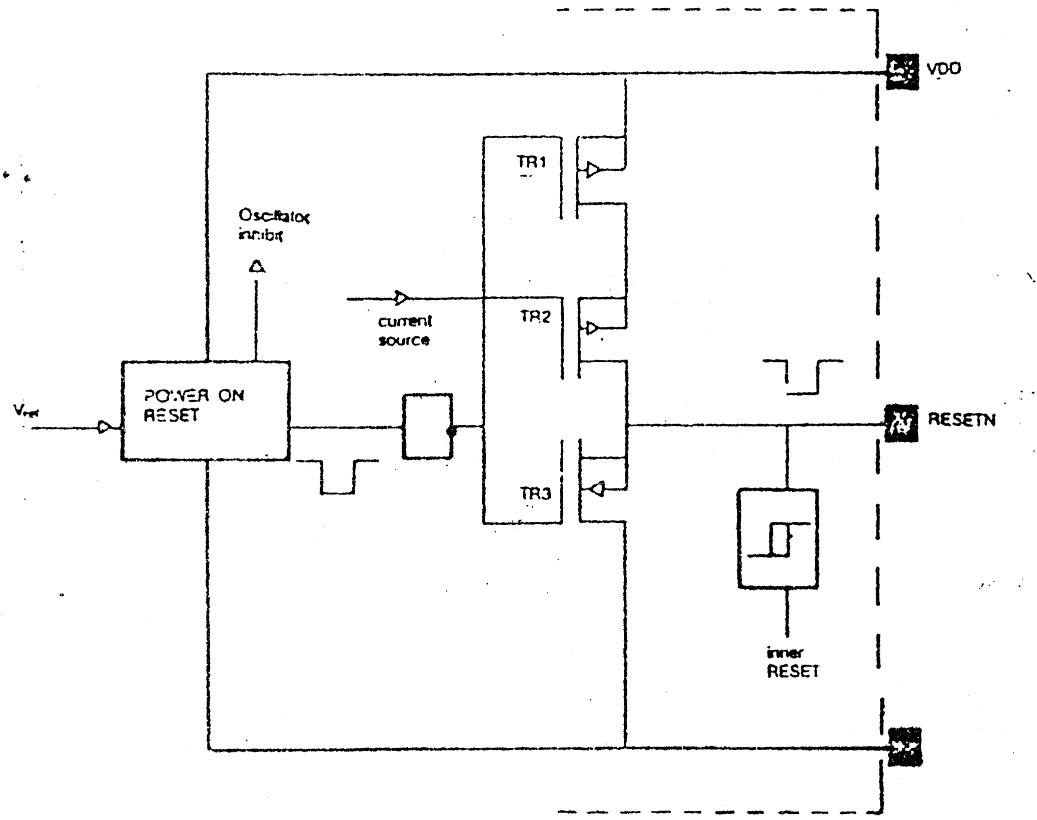

VDD
TR1
Oscillator inhibit
current source
TR2
POWER ON RESET
V_{ref}
RESETN
TR3
inner RESET

Fig. 2 · 1 RESETN configuration.

VDD has fast rise time, then no external components are required.

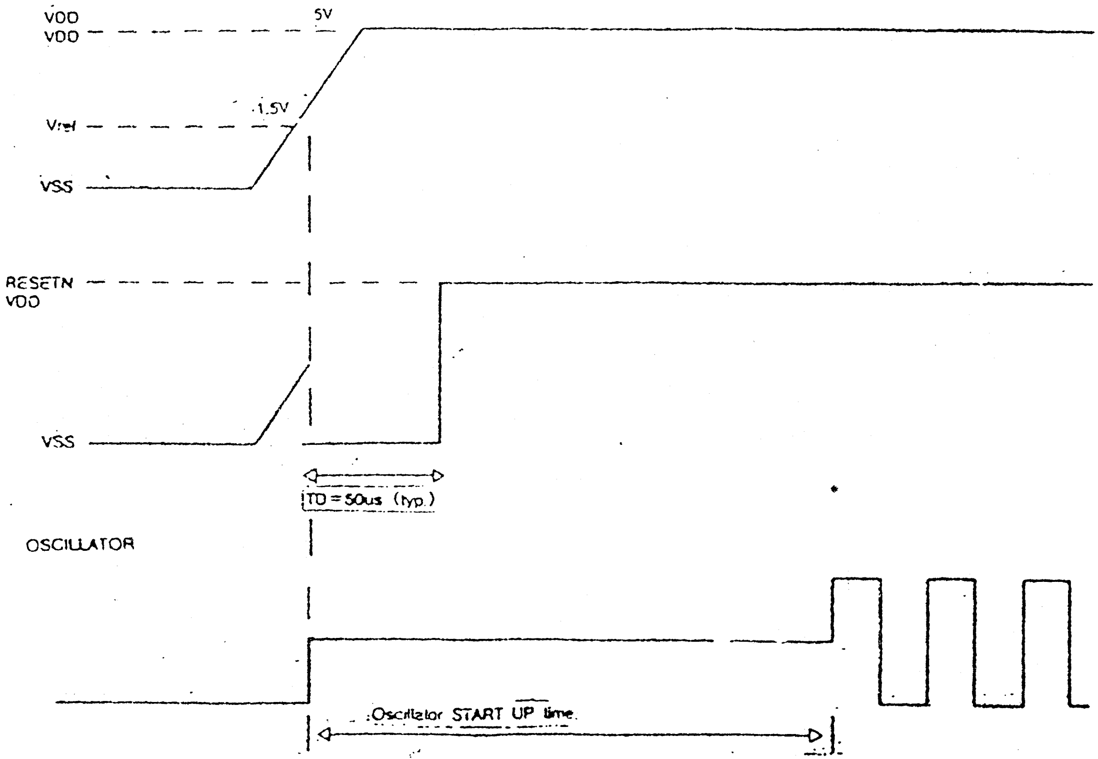

VDD
VDD
5V
1.5V
Vref
VSS
RESETN
VDD
VSS
TD = 50us (typ.)
OSCILLATOR
Oscillator START UP time

Fig. 2. 2 RESETN with fast rising VDD.

3. If VDD has a such a slow rise time that at t_{vref}+TD, the supply voltage is still less than the minimum operation voltage (Vmin) external components (RC-network) are required. (Fig 2.3).
In order to ensure a correct RESET/RC must-be >= 8*TVDD (Fig 2.4.)

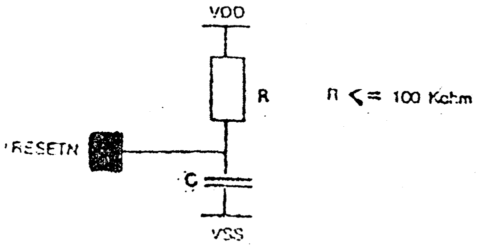

VDD
R
R <= 100 Kohm
RESETN
C
VSS

Fig. 2.3 External components for RESETN pin.

VDD rises slow, external components like in fig. 2.3. are required.

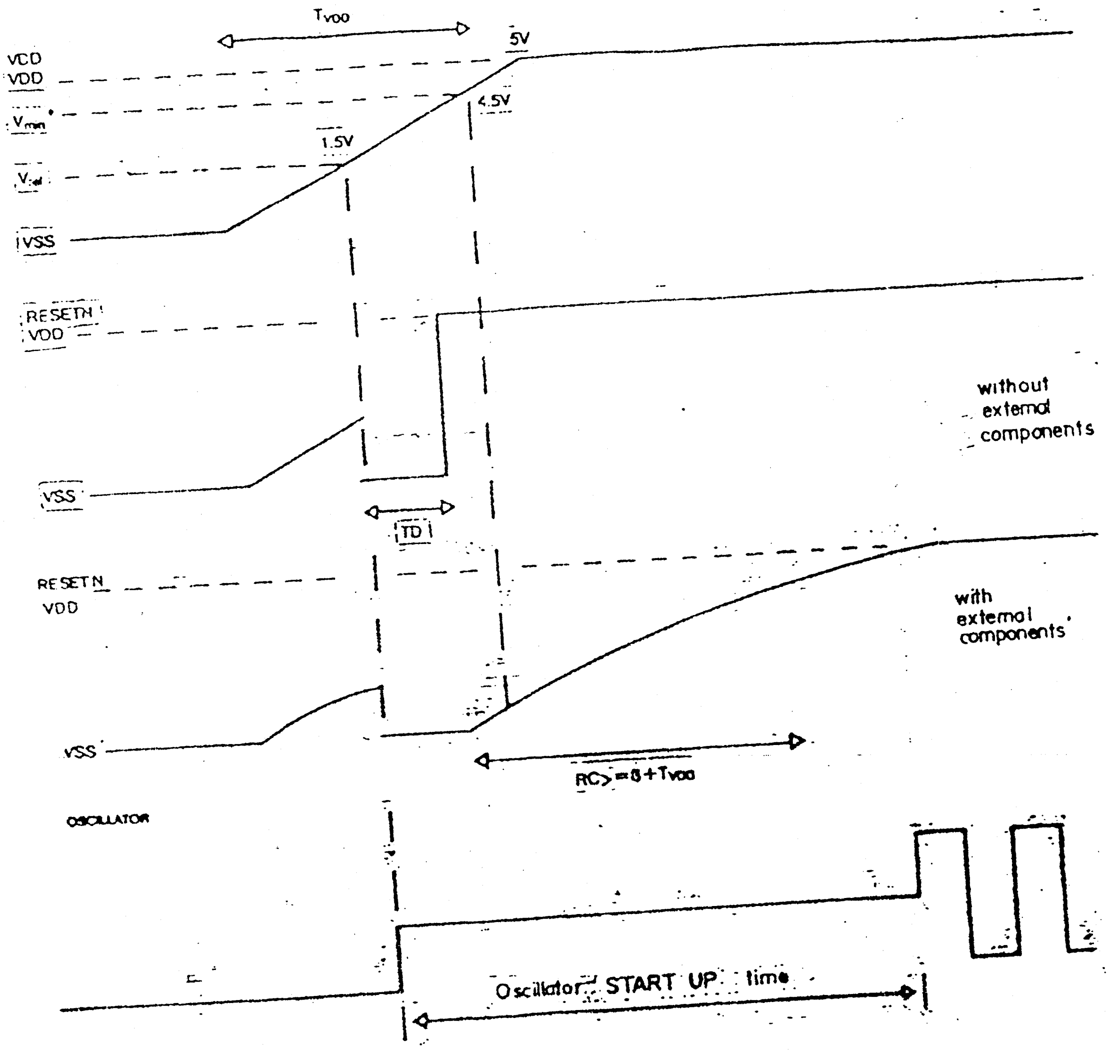

Tvdd
5V
VCD
VDD
Vmin
4.5V
1.5V
VSS
RESETN
VDD
without external components
VSS
TD
RESETN
VDD
with external components
VSS
RC>=5+Tvdd
OSCILLATOR
Oscillator START UP time

Fig. 2.4 RESETN with slow rising VDD.

4-2. Test (PIN 30)

This pin is used to set the chip in out of 3 modes, and therefore has 3 levels.

GND : Normal Operation
Vdd : Emulation mode
> 1.8 X Vdd :Test mode

4-3. Analog Control (PIN 2~PIN 6)

These PWM outputs generate pulse patterns with a repetion time of $f_{PWM}/64$. The analog value is determined by the ratio of the High time and repetion time. A d.c. voltage proportional to the PWM control setting is obtained by means of an external integration net work. (Low Pass Filter)

4-4. AFC Input (PIN 9)

This pin is intented to measure the level of the Automatic Frequency contról signal. This is done by comparing the AFC signal with the output of the 3-bit D/A converter as shown in Fig.below. The DAC analog switchs select one of 8 resistor taps of resistor chain that is connected between Vdd and Vss.

The AFCC signal then can be testen to check whether the AFC input is higher or lower than the DAC level. The AFC input shares the pin with a DP17 I/O line under control of the AFCE bit (AFC enable/disable).

AFCE : 0 : disable comparator and 3-bit D/A, enable DP17 output buffer

1 : enable comparator and 3-bit D/A, disable DP17 output buffer

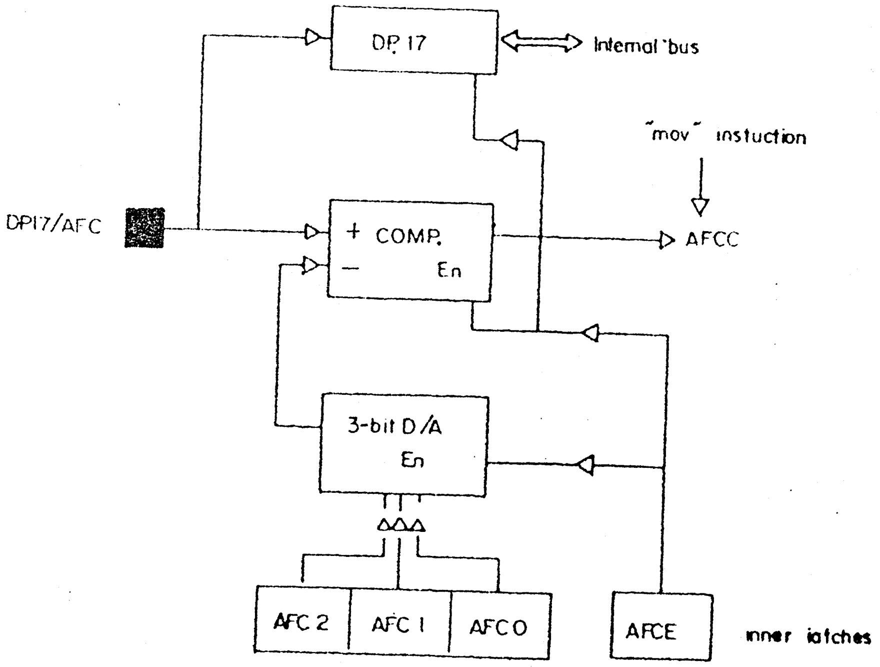


Fig. AFC circuit.

AFC2 AFC1 AFC0	Vref	Vref (Vdd=5.0 V)
0 0 0	Vdd*0.125	0.625 V
0 0 1	Vdd*0.25	1.250 V
0 1 0	Vdd*0.375	1.875 V
0 1 1	Vdd*0.5	2.500 V
1 0 0	Vdd*0.625	3.125 V
1 0 1	Vdd*0.75	3.750 V
1 1 0	Vdd*0.875	4.375 V
1 1 1	Vdd	5.000 V

Table. Vref as function of AFC2. .0.

4-5. I/O ports (PIN 13~20,PIN 7,8,10,11)

PIN 13~20 (P00-P07) have extra output sinking capability (10 mA at Vol=0.5V) so it can be used as LED driver.
Three different options are possible.

1. standard I/O with switched pull-up current source
2. open drain I/O
3. push-pull output

The output stage of a port consist of 4 transistors:

TR1 : N-Channel transistor for "sink"
TR2 : P-Channel transistor for "boost-up"
TR3 : P-Channel transistor for "pull-up"
TR4 : P-Channel transistor for "constant current"

(For more details in I/O ports in the core specification see 8 bit microcontrollers user manual.)

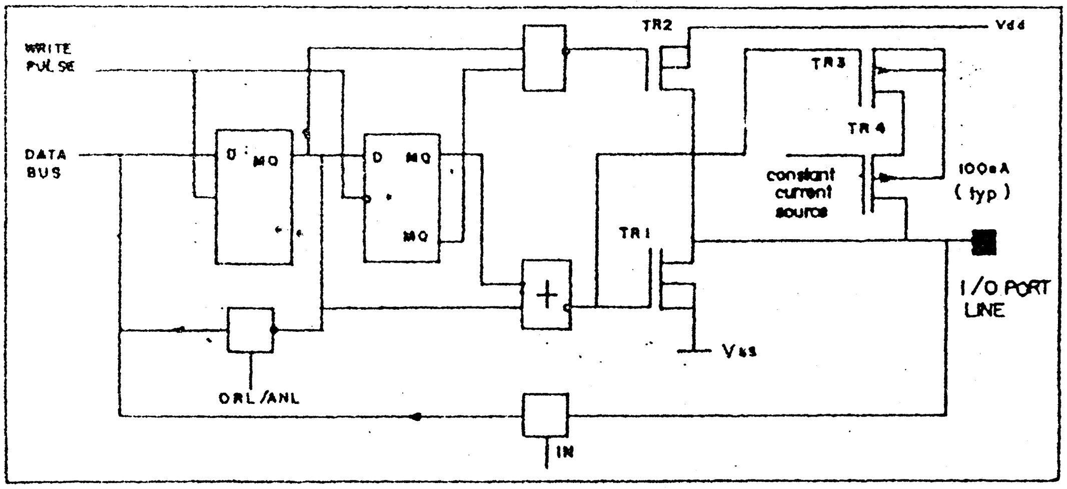

WRITE PULSE
DATA BUS
D MQ
D MQ
MQ
MQ
TR2
Vdd
TR3
TR4
constant current source
100μA (typ)
TR1
+
I/O PORT LINE
Vss
ORL/ANL
IN

Fig. 1. Standard output with switched pull-up current source.

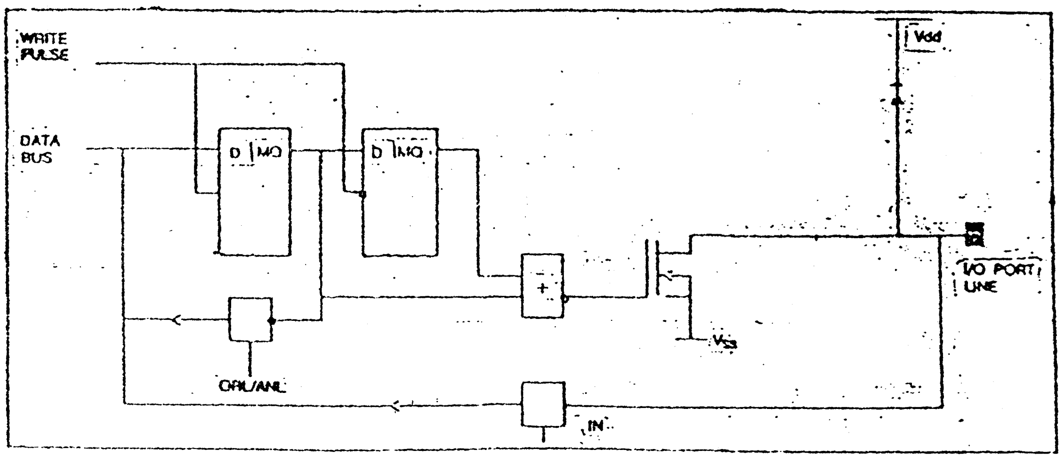

WRITE PULSE
DATA BUS
D MQ
D MQ
Vdd
+
I/O PORT LINE
Vss
ORL/ANL
IN

Fig. 2. Open drain type I/O

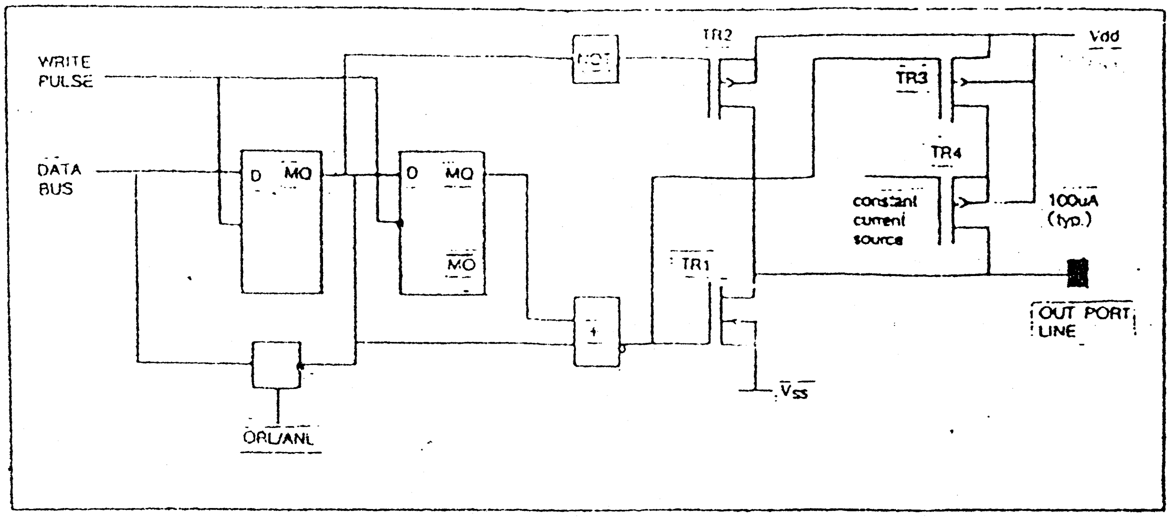

WRITE PULSE
DATA BUS
D MQ
D MQ
MQ
NOT
+
ORL/ANL
TR2
TR1
TR3
TR4
Vdd
Vss
constant current source
100uA (typ.)
OUT PORT LINE

Fig. 3. Push-Pull type output.

4-6. VOB and VO3 (PIN 25,24)

These pins are outputs only, they do not share a pin with a DPxx line. The confiruration of three pins are push-pull as shown in Fig. After Reset, VO3 and VOB are LOW.

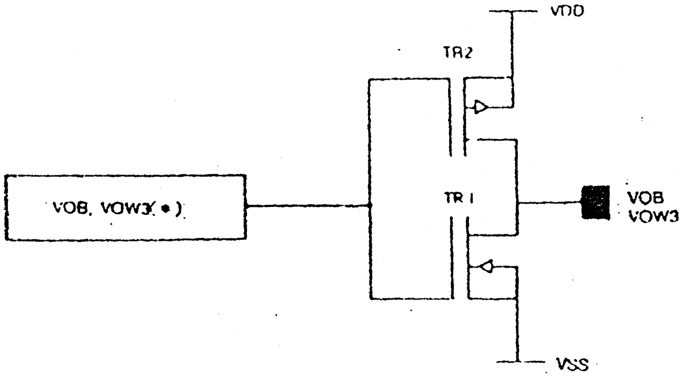

VDD
TR2
VOB, VOW3(*)
TR1
VOB
VOW3
VSS

Fig . Push Pull outputs VOB and VOW3.
(*) : Outputs of derivative (DOS) block

5. DOS (Display On Screen)

5-1. Features

- Display format 2 rows X 16 character
- 48 type of characters in ROM
- black box background (software controlled)
- 4 character sizes under for each line (software controlled)
- software controlled vertical & horizontal display position
- 4 out of 7 colors possible on one screen
- Half-dot rounding (software controlled)
- 9 or 13 dot character height (software controlled)
- 6 or 8 dot character width (software controlled)

5-2. Horizontal display position control

The horizontal position counter is increased every DOSC cycle and is reset by the HSYNCN (PIN 26) signal.

5-3. Vertical display position control

The vertical position counter is increased every HSYNCN cycle and is reset by the VSYNCN (PIN 27) signal.

6. Application Information

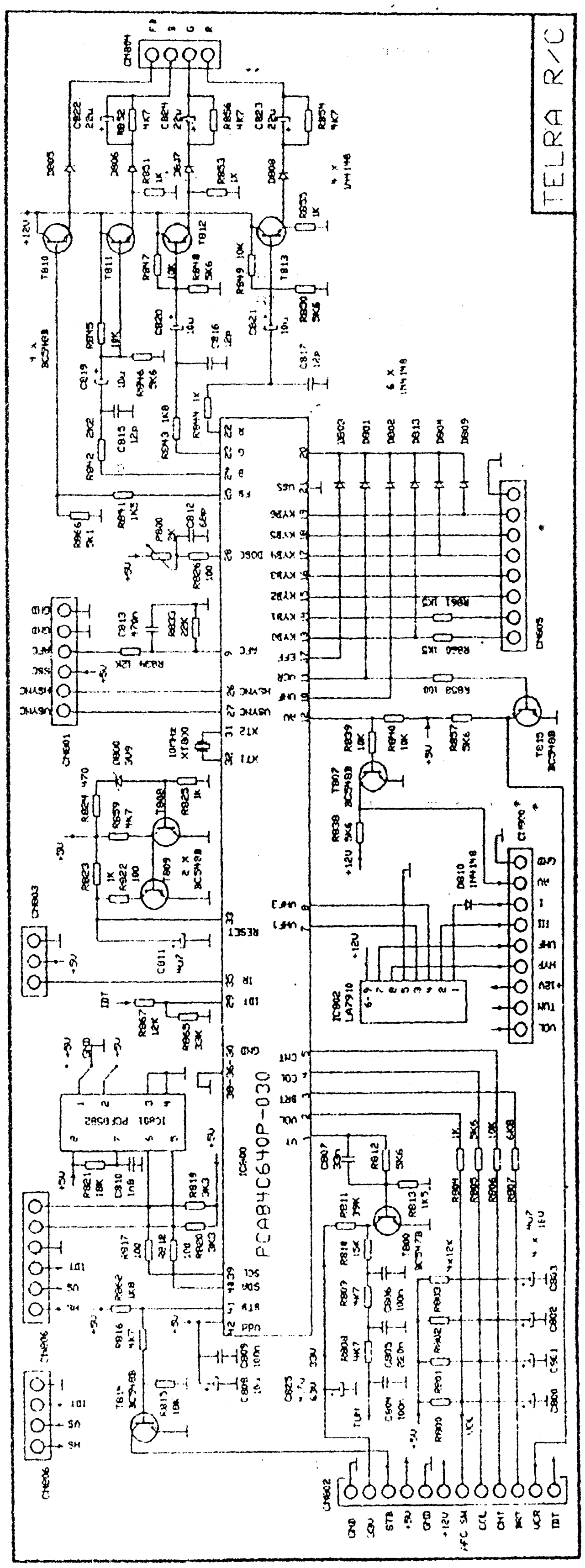
PIN 42 : Supply

voltage : 4.5~5.5 V (typ. 5.0 V)
current : 16 mA..max.

- **I/O Terminal 1:** PIN 7,8,10,11,12 (P.10~P14). PIN 1 (DP00)
  PIN 2~6 (DP01~DP05), PIN 40,39 (DP06. DP07)
  PIN 23 (DP15), PIN 22 (DP16), PIN 9 (DP17)

  input voltage High ; 3.5~Vdd
  Low ; Vss~1.5 V
  pull-up outptut current ; min. 40 uA (at Vol =3.5 V)
  max. 400 uA (at Voh = 0 V)
  typ. 2.5 mA (at Voh = 4.5 V)
  output voltage Low ; max. 0.5 V (at Iol = 2.5 mA)
  input leakage current ; max. - 10 uA
- **I/O Terminal 2:** PIN 13~ PIN 20 (P00~P07)
  input voltage High ; 3.5~ Vdd
  Low ; Vss ~1.5 V
  pull-up output cuttent ; min. 40 uA (at Vol = 3.5 V)
  max. 400 uA (at Voh = o V)
  typ. 2.5 mA (at Voh = 4.5 V)
  output voltage Low ; max. 0.5 V (at Iol = 2.5 mA)
  input leakage current ; max. ± 10 uA
- **I/O Terminal 3:** PIN 33 (Reset)

  input vlotage High ;3.5 V~Vdd
  Low ;Vss ~ 1.5 V
  input current ; typ. 10uA (at Vin =1.5 V)
  output voltage High ; typ. 4.5 V (at Ioh =0.5 mA)
  output voltage Low ; typ. 0.5 V (at Ioh = 500 uA)
- **Output Terminal 1:** PIN 25, PIN 24~PIN 22 (VOB, VOW 3~VOW1)
  output voltage High ; min. 4.5 V
  Low ; max. 0.5 V
- **Input Terminal 1:** PIN 35,29 (INTN T0.T1)
  input voltage High ; 3.5 V~ Vdd
  Low ; Vss ~ 1.5 V
  input leakage current : ± 10 uA (at Vin = 0~5 V)
- **Input Terminal 2:** PIN 26,27 (HASYNC, VSYNC)
  input voltage High ; 3.5 V ~ Vdd
  Low ; Vss ~ 1.5 V
  input leakage current ;± 10 uA (at Vin = 0~5 V)


TELRA R/C
PCA84C640P-030
IC800
IC801 PCF8582
IC802 LA7910
CN801
CN802
CN803
CN804
CN805
CN806
T810
T811
T812
T813
T815
4 x BC548B
6 x 1N4148
XT800 10MHz
GND
SDA
SCL
+5V
+12V
AFC
VSYNC
HSYNC
RESET
KYB0
KYB1
KYB2
KYB3
KYB4
KYB5
KYB6
R
G
B
FB
IR
IDT
VCR
ON
STB
AFC SW
CVL
CNT
BRT
VOL
TUN

2. SEMICONDUCTOR SPECIFICATION (LA7910)

The LA7910 is an IC for tuner band selection of electronic tuning type television set. This IC is used for producing the VHF channel "L" band power supply/UHF channel "H" power supply/UHF channel power supply for tuner and the CATV power supply according to the band select signal of 2 inputs.

Functions

- VHF "L" band power supply output.
- VHF "H" band power supply output.
- UHF power supply output.
- CATV power supply output.

Features

- 2 inputs and 4 outputs.
- Output low saturation voltage: 0.25V typ., Io = 60mA.
- Compact 9-pin single-end package.

Maximum ratings at Ta = 25°C

Parameter			Unit
Maximum supply voltage	V_9 max.	15	V
Maximum load current	I_1 max., I_2 max., I_7 max., I_8 max.	–60	mA
Maximum supply current Vcc2	I_6 max.	10	mA
Allowable power dissipation	Pd max.	200	mW
Operating temperature	Topg	–20 to +85	°C
Storage temperature	Tstg	–55 to +125	°C
Input current	I_3 max., I_4 max.	2	mA

Electrical characteristics at Ta = 25°C

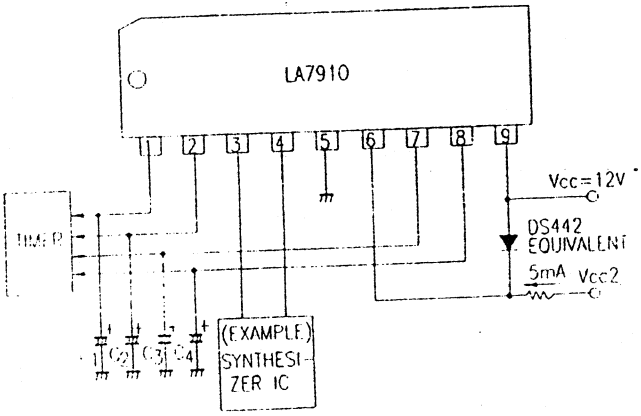
Parameter			Min.	Typ.	Max.	Unit
Dissipation current	I_1, I_2, I_7, I_8				60	mA
Output saturation voltage		$V_9 = 12V$, $I_6 = 5mA$, $I_o = 60mA$	0	0.25	0.7	V
Input "H" level threshold voltage	VTH				3.0	V
Input "L" level threshold voltage	VTL		0.8			V
Output leak current	I_1, I_2, I_7, I_8	Ta≤70°C			50	µA

Truth table

Input		Output			
Pin 3	Pin 4	Pin 1	Pin 2	Pin 7	Pin 8
L	L	H	Z	Z	Z
H	L	Z	H	Z	Z
L	H	Z	Z	H	Z
H	H	Z	Z	Z	H

Z: High impedance
Input threshold voltage:
VTL = 0.8V, VTH = 3V.

Application circuit



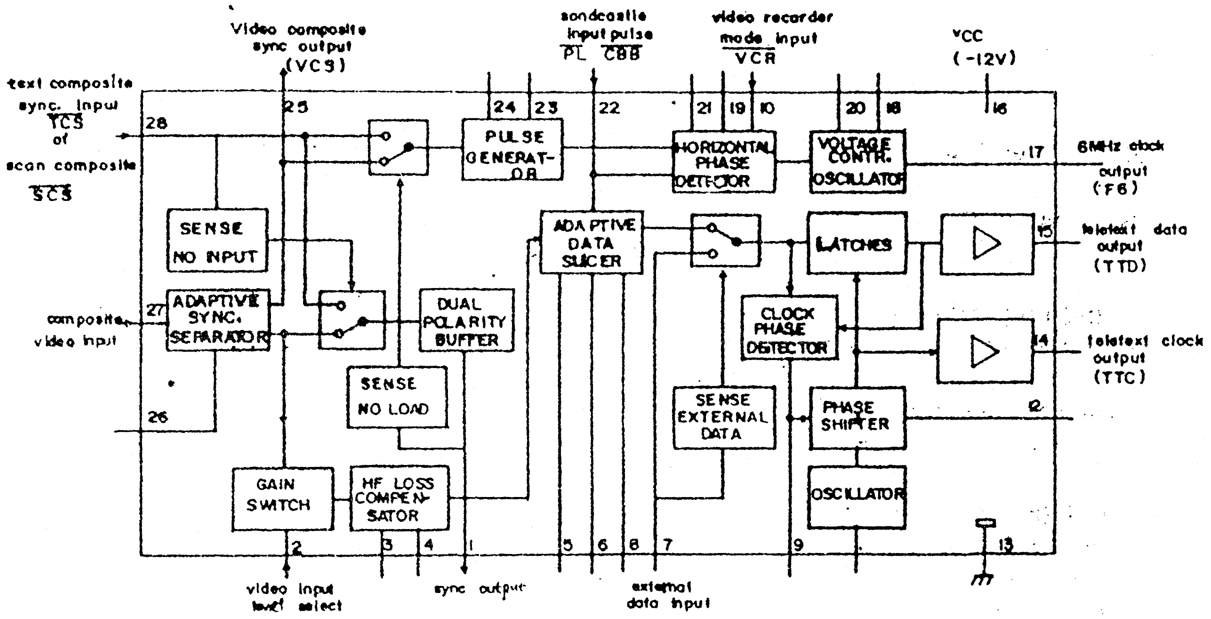
Proper cares in using the IC

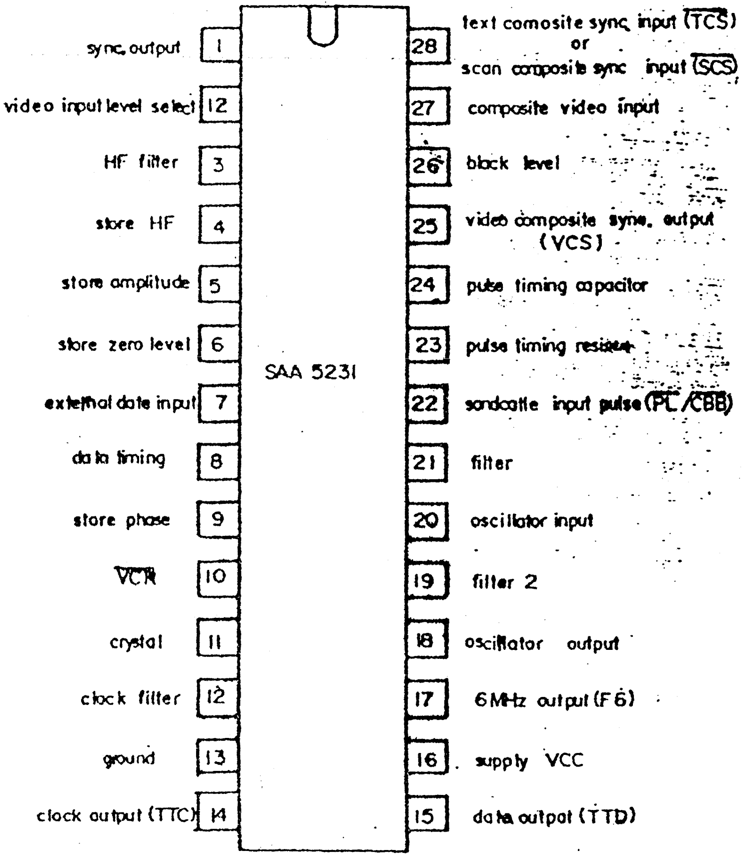
1. When using a capacitive load, connect a diode across pins 6 and 9 as shown the above.
2. The value of load capacitors C1, C2, C3, C4 must not exceed 22µF.

TELETEXT CIRCUIT

Teletext Video Processor (SAA 5231, IC 1)

It seperates Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television sync.


Video composite sync output (VCS)
sandcastle input pulse PL CBB
video recorder mode input VCR
VCC (-12V)
text composite sync. input TCS or scan composite SCS
28
25
24
23
22
21
19
10
20
18
16
PULSE GENERATOR
HORIZONTAL PHASE DETECTOR
VOLTAGE CONTR. OSCILLATOR
17
6MHz clock output (F6)
SENSE NO INPUT
ADAPTIVE DATA SLICER
LATCHES
15
teletext data output (TTD)
27
composite video input
ADAPTIVE SYNC. SEPARATOR
DUAL POLARITY BUFFER
CLOCK PHASE DETECTOR
14
teletext clock output (TTC)
SENSE NO LOAD
SENSE EXTERNAL DATA
PHASE SHIFTER
12
26
GAIN SWITCH
HF LOSS COMPENSATOR
OSCILLATOR
2
3
4
1
5
6
8
7
9
13
video input level select
sync output
external data input


SAA 5231
sync output 1
video input level select 12
HF filter 3
store HF 4
store amplitude 5
store zero level 6
external data input 7
data timing 8
store phase 9
VCR 10
crystal 11
clock filter 12
ground 13
clock output (TTC) 14
28 text comosite sync input (TCS) or scan composite sync input (SCS)
27 composite video input
26 black level
25 video composite sync. output (VCS)
24 pulse timing capacitor
23 pulse timing resistor
22 sandcastle input pulse (PL/CBB)
21 filter
20 oscillator input
19 filter 2
18 oscillator output
17 6MHz output (F6)
16 supply VCC
15 data output (TTD)

■ Application Information

PIN 1 : Sync. output to TV
a load (R16) resister to GND ; positive-going sync.
voltage 1.0~2.0 V (typ. 1.4 V)
a load (R16) resister to 12 V ; negative-going sync.
voltage 9.0~11.9 V (typ. 10.1 V)

PIN 2 : Video input level select

This pin has internal pull-up resister so that the larger input is automatically selected if there is no connection to this pin.

Low (0~0.8 V) ; 1Vp-p video input (PIN 27) is selected.
Float or High (2.0~5.5) ;2.5 Vp-p video input (PIN 27) is selected.

PIN 3 : HF filter (RF level stabilizer)
The video signal for the HF-loss compensator is filtered by C22.

PIN 4 : Store HF (RF level stavilizer)
The HF amplitude is stored by C21.

PIN 5 : Store amplitude
The amplitude for the adaptive data slicer is stored by C19.

PIN 6 : Store zero level
The zero level for adaptive data slicer is stored by C18.

PIN 7 : External teletext data input (already seperated)
Not Used

PIN 8 : Data timing
Adaptive C17 is connected to this pin for timing of adaptive data slicer.

PIN 9 : Store clock phase
The output signal from the clock phase detector is stored by C16.

PIN 10 : Video tape recorder mode (VCR)
Not Used
VCR mode on (LOW) ; 0~0.8
off (High) ; 2.0~Vcc

PIN 11 : Crystal

A 13.875 Mhz crystal (X1) , 2Xteletext data rate, connected in series with C15 capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6.9375 Mhz clock signal.

PIN 12 : Clock filter

A filter (C14 parallel with L1) for the 6.9375 Mhz clock signal is connected.

PIN 13 : Ground

PIN 14 : Teletext clock output (TTC)

clock output for CCT (Computer Controlled Teletext)
AC voltage ; 2.5~4.5 Vp-p (typ. 3.5 Vp-p)
dc voltage ; 3.0~5.0 V (typ. 4.0 V)
load capacitance ; 40 pF max.
rise and fall times : 20~45 nS (typ. 30 nS)

PIN 15 : Teletext data output (TTD)

data output for CCT
AC voltage ; 2.5~4.5 Vp-p (typ. 3.5 Vp-p)
dc voltage ; 3.0~5.0 V (typ. 4.0 V)
load capacitance ; 40 pF max.
rise and fall times ; 20~45 nS (typ. 30. nS)

PIN 16 : Supply Vcc
voltage ; 10.8~13.2 V (typ.12 V)
current ; 50~105 mA (typ. 70 mA)

PIN 17 : Clock output (F6)
6Mhz clock output for timing and sand castle
voltage ; 1~3 V (typ. 2 V)

Ac and dc output voltage range ; 4.0~8.5 V
load capacitance ; 40 pF max.
rise and fall times ; 20~40 nS

PIN 18 : Oscillator output (6 Mhz)

A series resonant circuit (TC 1, R4, X2) is connected between this pin and PIN 20 to control the nominal frequency of the VCO.

PIN 19 : Filter 2 (RC combination)

A filter (C9) with short time constant during VTR or asynchronous operation is connected to this pin for the horizontal phase detector.
It is used in the video recorder mode and while the loop is locking up.

PIN 20 : Oscillator input (6 Mhz)
See PIN 18

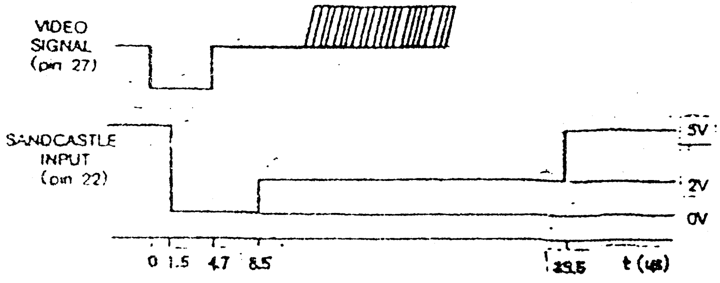
PIN 21 : Filter 1 (RC combination)

A filter (C7) with long time constant is connected to this pin for the horizontal phase detector.

PIN 22 : Sand castle input pulse ($\overline{PL}$/$\overline{CBB}$)

This input accepts a sand castle waveform, which is formed from PL (phase locking pulse) and CBB

(blanking pulse) from the CCT>
PL on (Low) ; 0~3 V
off (High) ; 3.9~5.5 V
CBB on (Low) ; 0~0.5 V
off (High) ; 1.0~5.5 V



Sandcastle waveform and timing.

PIN 23 : Pulse timing resister (to determine time constant for PLL pulse generator)
The current for the pulse generator is defined by R3.

PIN 24 : Pulse timing capacitor (to determine time constant for PLL pulse generator)
The timing of the pulse generator is determined by C6.

PIN 25 : Video composite sync. output (VCS)
This output signal is for CCT.
voltage Low ; 0~0.4 V
High ; 2.4~5.5 V

PIN 26 : Black level
The black level for the adaptive sinc. seperator is stored by C5.

PIN 27 : Composite video signal input (CVS)
Composite video signal is input via C13 clamping (coupling) capacitor to the adaptive sync. seperator.

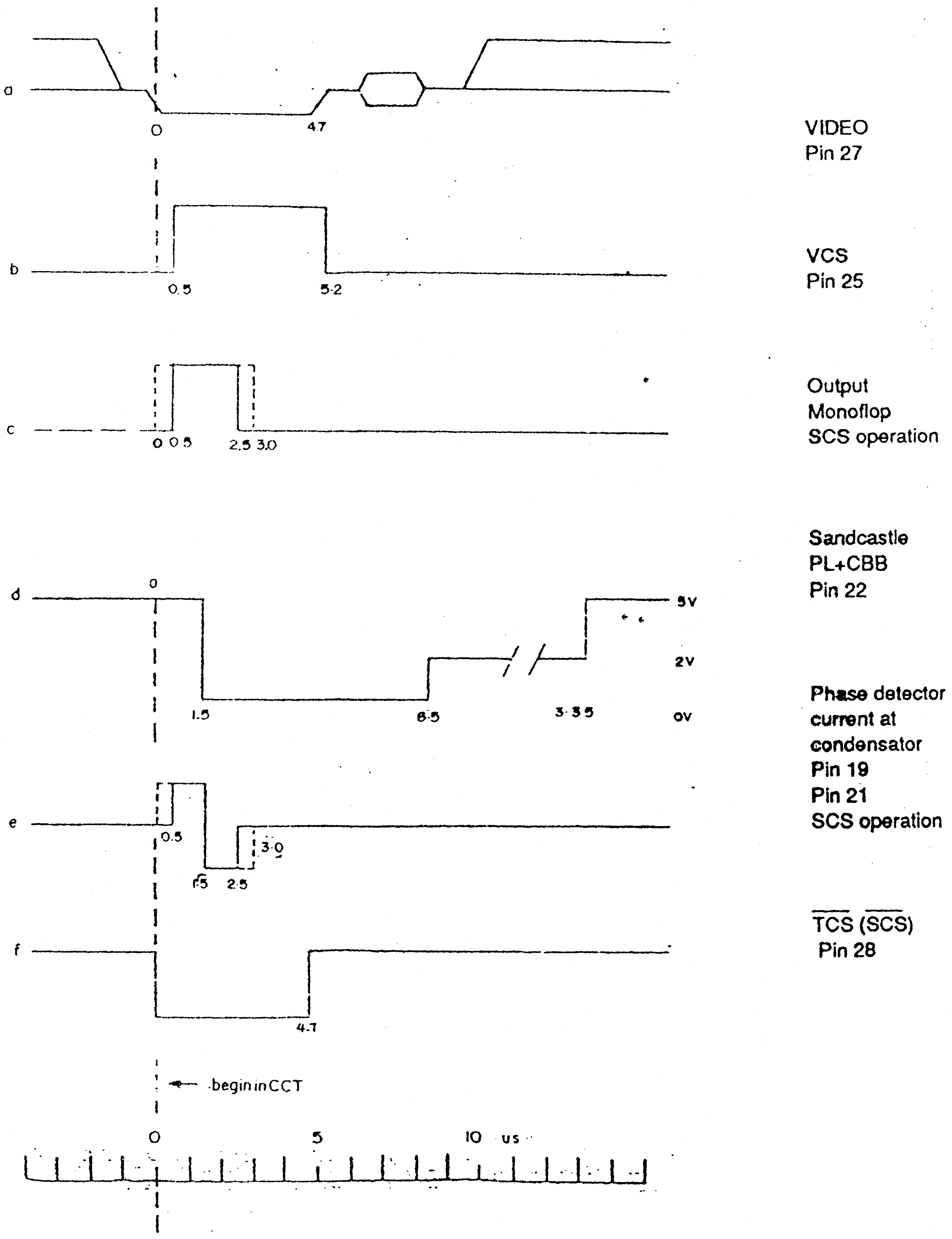
video input select	Low (PIN 2) ;	0.3~0.7 V (typ. 0.46 V)
		0.7~1.4 Vp-p (typ. 1 Vp-p)
	High (PIN 2) ;	0.75~1.75 V (typ. 1.15 V)
		1.15~3.5 Vp-p (typ. 2.5 Vp-p)

PIN 28 : Text Composite Sync. input ($\overline{TCS}$) / Scan Composite Sync. input ($\overline{SCS}$)

TCS is input from CCT (during TXT play-back)
voltage Low ; 0~0.8 V
High ; 2.0~7.0
current ; -40~-100 uA (typ. -70 uA)

SCS from external sync. circuit (when PIN 1 is open)
voltage Low ; 0~1.5 V
High ; 3~7.0 V

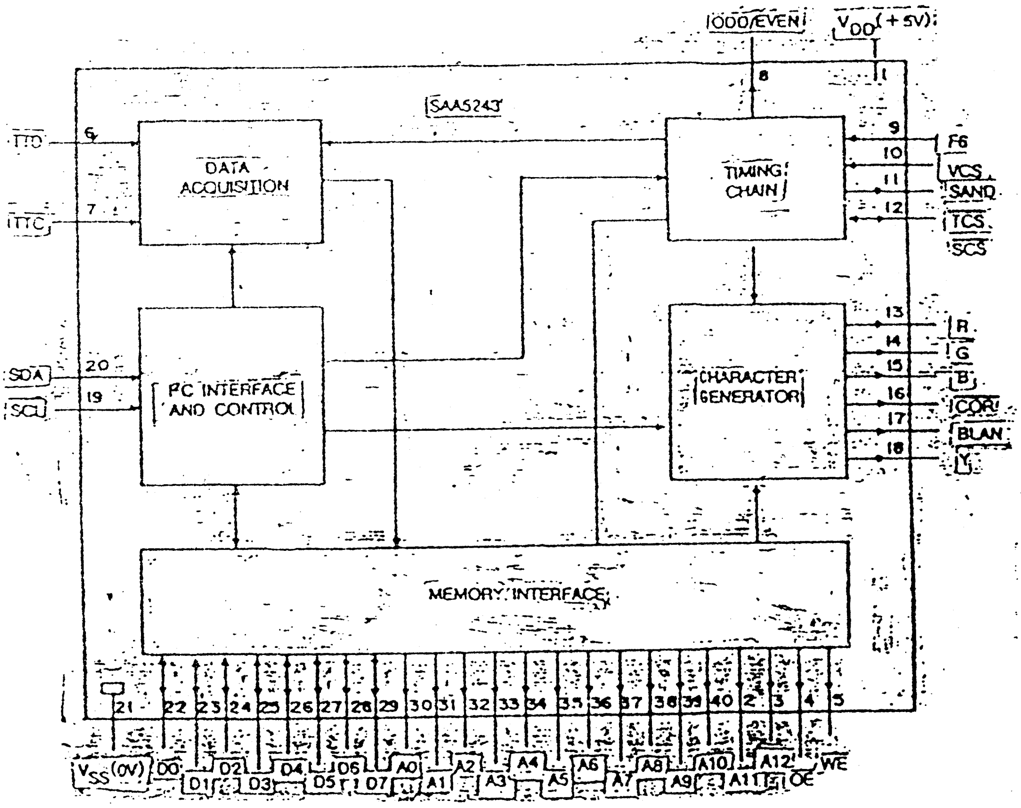
■ TIMING DIAGRAMS


a
0
4.7
VIDEO
Pin 27
b
0.5
5.2
VCS
Pin 25
c
0 0.5
2.5 3.0
Output
Monoflop
SCS operation
Sandcastle
PL+CBB
Pin 22
d
0
5V
2V
1.5
6.5
3-3.5
0V
Phase detector
current at
condensator
Pin 19
Pin 21
SCS operation
e
0.5
3.0
1.5
2.5
$\overline{TCS}$ ($\overline{SCS}$)
Pin 28
f
4.7
begin in CCT
0
5
10 us

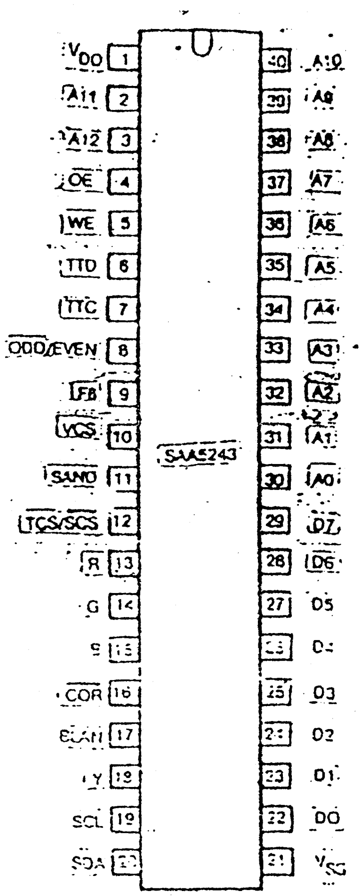
Enhanced Computer Controlled Teletext (ECCT,SAA 5243. IC 2)

This is MOS N-channel teletext processor which generate characters

- can store 8 teletext pages
- acquire 4 pages simultaneously
- acquisition during vertical blanking interval 3 to 22 or full channel (all line) data
- direct interface up to 8K bytes static RAM
- 25th display row for software generated status message
- standard I²C bus slave transceiver


ODD/EVEN
V_{DD} (+5V)
8
1
SAA5243
TTD
6
TTC
7
DATA ACQUISITION
TIMING CHAIN
9
10
11
12
F6
VCS
SAND
TCS
SCS
SDA
SCL
20
19
I²C INTERFACE AND CONTROL
CHARACTER GENERATOR
13
14
15
16
17
18
R
G
B
COR
BLAN
Y
MEMORY INTERFACE
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
2
3
4
5
V_{SS} (0V)
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
OE
WE

Block diagram.


VDD 1
A11 2
A12 3
OE 4
WE 5
TTD 6
TTC 7
ODD/EVEN 8
LFB 9
VCS 10
SAND 11
TCS/SCS 12
R 13
G 14
B 15
COR 16
BLAN 17
Y 18
SCL 19
SDA 20
40 A10
39 A9
38 A8
37 A7
36 A6
35 A5
34 A4
33 A3
32 A2
31 A1
30 A0
29 D7
28 D6
27 D5
26 D4
25 D3
24 D2
23 D1
22 D0
21 VSS
SAA5243

■ Application Information

PIN 1 (Vdd) : Supply

voltage ; 4.5~5.5 V (typ. 5.0 V)
current ; 270 mA max. (typ. 160 mA)

PIN 2,3,40 (A11,A12,A10) : Chapter address output

Three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.

voltage Low ; 0~0.4 V (at Iol = 1.6 mA)
High ; 2.4~Vdd (Ioh =0.2 mA)
rise and fall time ; 50 nS max. (between 0.6~2.2 V)
load capacitance ; 120 pF max.

PIN 4 ($\overline{OE}$) : Output Enable

Active low output signal used to control the reading of data of the external RAM.
It occurs continuously at a 1 Mhz rate.

vlotage Low ; 0~0.4 V (at Iol = 1.6 mA)
High ; 2.4~Vdd (Ioh = 0.2 mA)
rise and fall times ; 50 nS max. (between 0.6~2.2 V)
load capacitance ; 120 pF max.

PIN 5 ($\overline{\text{WE}}$) : Write Enable

Active low output signal used to control the writing of data to the external RAM.
It occurs for a valid write cycle only and is interleaved with a read cycle.

vlotage Low ; 0~0.4 V (at Iol = 1.6 mA)
High ; 2.4~Vdd (Ioh = 0.2 mA)
rise and fall times : 50 nS max. (between 0.6~2.2 V)
load capacitance ; 120 pF max.

PIN 6 (TTD) : Teletext Data

Input from the IC 1 (video input processor)
It is clamped to Vcc for 4 to 8 uS of each television line to maintain the correct d.c. level following the external a.c. coupling.

external coupling capacitor (C12) ; 50 nF max.
input voltage ; 2.0~7.0 Vp-p
input data rise and fall time ; 10~80 nS
input data set up time ; 40 nS min.
input data hold time ; 40 nS min.
input leakage current ; 20 nA max.
input capacitance ; 7 pF max.

PIN 7 (TTC) : Teletext Clock

6.9375 Mhz clock input from the IC 1
It is intenally a.c. coupled to an active clamp input buffer.

input DC voltage ; -0.3~10.V
input AC voltage ; 1.5~7.0 Vp-p
input rise and fall time ; 10~80 nS
input leakage current ; 20 uA max.
input capacitance ; 7 pF max.

PIN 8 ($\overline{\text{ODD}}$/EVEN) : Odd/Even

- For interlaced mode, the output changes once per field at 2 uS before the end of line 311 (624).
The output is high for even fields and low for odd fields.

voltage Low ; 0~0.4 V (at Iol = 0.4 mA)
High ; 2.4~Vdd (at Ioh = 0.2 mA)
output rise and fall time ; 100 nS max.
load cpacitance ; 50 pF max.

PIN 9 (F6) : Character display clock

6 Mhz clock input from the IC 1.
It is intenally a.c. coupled to an active clamp input buffer.
input DC voltage ; -0.3~10 V

input AC voltage ; 1.0~7.0 Vp-p
clock rise and fall time ; 10~80 nS
input capacitance ; 7 pF max.

PIN 10 (VCS) : Video Coposite Sync.

Input from the IC 1 derived from the incoming video signal.
Sync. pules are active high.

Input voltage Low ; 0~0.8 V
High ; 2.0~Vdd
rise and fall time ; 500 nS max.
input leakage current ; 10 uA max.
input capacitance ; 7 pF max.

PIN 11 (SAND) : Sandcastle

3 level sandcastle output to the IC 1 containing the phase locking and color burst blanking information.
output voltage Low ; 0~0.25 V (at Iol = 0.2 mA)
Intermediate ; 1.1~3.1 V (at Iol = ± 10 uA)
High ; 4.0~Vdd (at Ioh = 0~10 uA)
output rise time ; 400 nS max. (at 0.4~0.9 V)
; 200 nS max. (at 3.3~3.8 V)
output fall time ; 50 nS max. (at 3,8~0.4 V)
load capacitance ; 30 pF max.

PIN 12 ($\overline{\text{TCS}}$/$\overline{\text{SCS}}$) : Text composite Sync. (output) /Scan Composite Sync. (input)

As an output an active low composite sync. waveform ($\overline{\text{TCS}}$) with interlaced or non-interlaced format which is fed to (IC 1) to drive the display timebases.
Alternatively this pin can act as an input for an active low composite sync. waveform ($\overline{\text{SCS}}$) to "slave" the display timing circuit.

input voltage Low ; 0~1.5 V
High ; 3.5~10 V
input rise and fall time ; 500 nS max.
input leakage current ; 10 uA max. (Vi = 0~10 V)
input capacitance ; 7 pF max.

output voltage low ; 0~0.4 V (at Iol = 0.4 mA)
High ; 2.4~Vdd (at Iol = 0.2 mA)
2.4~6V (at Iol = 0.1 mA)
output rise and fall time ; 100 nS max. (0.6 V~2.2 V)
load capacitance ; 50 pF max.

PIN 13,14,15 (R,G,B.) ; Red, Green, Blue

These 3 open drain outputs are the character video output signal to the television display circuits.
They are active high and contain character and back ground information.

output voltage Low ; 0~0.4 V (at Iol = 2 mA)
0~1.0 V (at Iol = 5 mA)
pull up voltage ; 6 Vmax.
output leakage current ; 10 uA max. (Vpu = 0~ 6 V)
output fall time ; 20 nS max. (load 1.2 K to 6 V)
load capacitance ; 25 pF max.

PIN 16 ($\overline{\text{COR}}$) : Contrast Reduction

open drain,active low output

Not Used

PIN 17 (BLAN) : Blanking
Open drain active high output which controls the blanking of the television picture for a normal text display and for a mixed display.

output voltage Low ; 0~0.4 V (at Iol = 2 mA)
0~1.0 V (at Iol = 5 mA)
pull up voltage ; 6 V max.
output leakage current ; 10 uA max. (Vpu = 0~6 V)
output fall time ; 20 nS max. (load 1.2 K to 6 V)
load capacitance ; 25 pF max.

PIN 18 (Y) : Character foreground

Open drain, active high video output signal containing all the foreground information **displayed** on a television screen.
(e.g. for driving a display printer)

Not Used

PIN 19 (SCL) : Serial Clock
Input signal which is the I^2C bus clock from the microcontroller.

input voltae Low ; 0~1.5 V
High ; 3~ Vdd
input clock frequency ; 100 Khz max.
rise and fall time ; 2 uS max.
input leakage current : 10 µ A max.
input capacitance ; 7 pF max.

PIN 20 (SDA) : Serial Data

I^2C bus data line
It is input/output function with an open drain output.
input voltage Low ; 0~ 1.5 V
High ; 3~Vdd
rise and fall time ; 2 uS max.
input leakage current ; 10 uA max.
input capacitance ; 7 pF max.

output voltage Low ; 0~0.5 V (at Iol = 3 mA)
output fall time ; 200 nS max. (between 3 V~1 V)
load capacitance ; 400 pF max.

PIN 21 (Vss) : Ground

PIN 22~29 (D0~D7) : 8 K data lines

3 state input/output pins which carry the data bytes to and from the external RAM.

input voltage Low ; 0~0.8 V
High ; 2.0~Vdd
input leakage current ; 10 uA max. (at 0~5V)
input capacitance ; 7 pF max.

output voltage Low ; 0~0.4 V (at Iol = 1.6 mA)
High ; 2.4~Vdd V (at Ioh = 0.2 mA)
output rise and fall time ; 50 nS max. (between 0.6~2.2 V)
load capacitance ; 120 pF max.

PIN 30~39 (A0~A9) : RAM Address

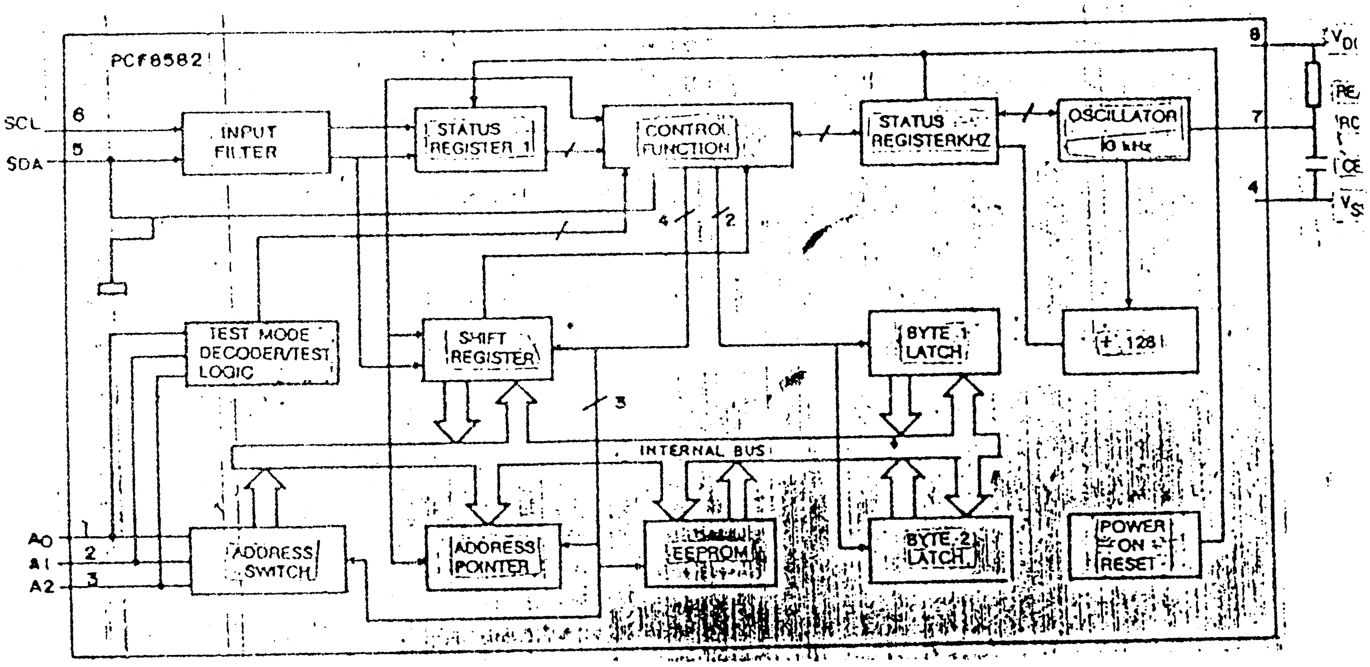
10 output signals that determine which bite location whithin a 1 K byte chapter of external RAM is accessed for any read or write cycle.

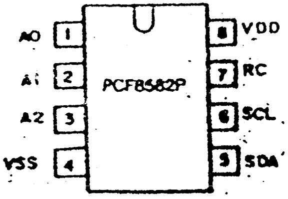
output voltage Low ; 0~0.4 V (at Iol = 1.6 mA)
High ; 2.4~Vdd (at Ioh = 0.2 mA)
output rise and fall time ; 50 nS max. (between 0.6~2.2 V)
load capacitance ; 120 pF max.

EEPROM (PCF 8582/ PCD 8582, IC 5)

EEPROM = E^2PROM (Electrically Erasable Programmable Read Only Memory)

Non-volatile storage of 2 K-bit organized as 256 X 8 bits for storage of preferred teletext page numbers in List mode.


PCF8582
SCL
SDA
6
5
INPUT FILTER
STATUS REGISTER 1
CONTROL FUNCTION
STATUS REGISTERKHZ
OSCILLATOR
10 kHz
8
7
4
VDD
RC
VSS
4
2
TEST MODE DECODER/TEST LOGIC
SHIFT REGISTER
BYTE 1 LATCH
÷ 128
3
INTERNAL BUS
A0
A1
A2
1
2
3
ADDRESS SWITCH
ADDRESS POINTER
EEPROM
BYTE 2 LATCH
POWER ON RESET


A0
A1
A2
VSS
1
2
3
4
PCF8582P
8
7
6
5
VDD
RC
SCL
SDA

- **Application Information**

PIN 1 (A0) :

PIN 2 (A1) : **address inputs/test**

PIN 3 (A2) : **mode select**

PIN 4 (Vss) : Ground

PIN 5 (SDA) : Serial Data

input voltage Low ; -0.3~1.5V
High ; 3~Vdd + 0.8 V
output voltage Low ; 0.4 V max. (Iol = 3mA, Vdd = 4.5 V)
High ;3~Vdd + 0.3 V
input capacitance ; 7 pF max.

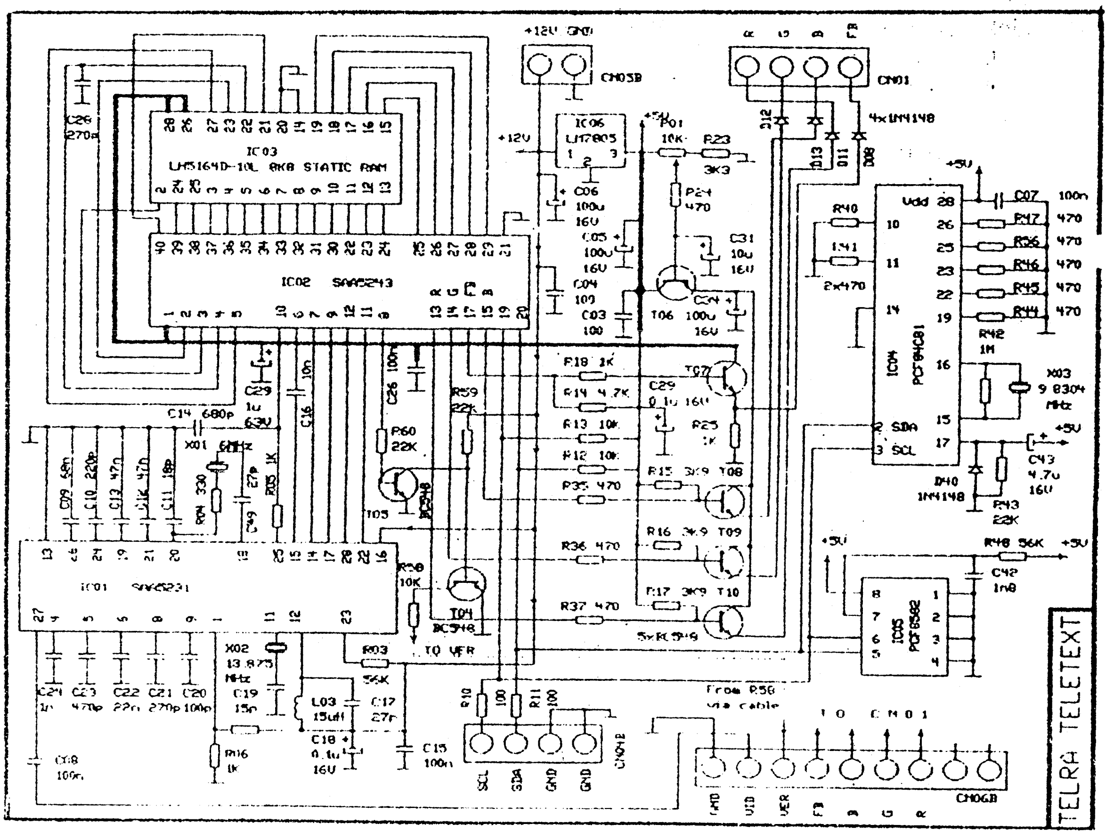
rise time ; 1 uS max.
fall time ; 300 nS max.

PIN 6 (SCL) : Serial CLock
input voltage Low ; -0.3~1.5 V
High ; 3~Vdd + 0.3 V
input leakage current ; 1 uS max.
input capcaitance ; 7 pF max.
clock frequency ; 0~100 Khz
rise time ; 1 uS max.
fall time ; 300 nS max.

PIN 7 (RC) : input for timer constant

PIN 8 (Vdd) : Supply

voltage ; 4.5~5.5 V (typ. 5.0 V)
current ; 0.4 mA max. (at Read time)
2.0 mA max. (at Write/Erase, Vdd max.)
10 uA max. (at Stand by, Vdd max.)


IC03
LH5164D-10L 8K8 STATIC RAM
IC02 SAA5243
IC01 SAA5231
IC04 PCF84C81
IC05 PCF8582
IC06 LM7805
CN03B
+12V GND
CN01
4x1N4148
D12
D13
D11
D08
Vdd
SDA
SCL
C26 270p
C06 100u 16V
C05 100u 16V
C04 100
C03 100
P01 10K
R23 3K3
P24 470
C31 10u 16V
C34 100u 16V
T06
C07 100n
R40
R41
2x470
R47 470
R56 470
R46 470
R45 470
R44 470
R42 1M
X03 9.8304 MHz
C43 4.7u 16V
D40 1N4148
R43 22K
R18 1K
R14 4.7K
C29 0.1u 16V
R25 1K
R13 10K
R12 10K
R15 3K9 T08
R35 470
R16 3K9 T09
R36 470
R17 3K9 T10
R37 470
5xBC549
T07
C29 1u 63V
C14 680p
X01 6MHz
C16
C26 100n
R59 22K
P60 22K
T05
BC548
T04
BC548
R58 10K
C09 68n
C10 220p
C13 47n
C1K 47n
C11 18p
R04 330
C49 27p
R05 1K
X02 13.875 MHz
C19 15p
L03 15uH
C17 27p
R03 56K
TO VER
C24 1n
C23 470p
C22 22n
C21 270p
C20 100p
C08 100n
R16 1K
C18 0.1u 16V
C15 100n
R10 100
R11 100
CN04B
SCL
SDA
GND
GND
From R58 via cable
TO CN01
CN06B
VID
VER
FB
+5V
R48 56K
C42 1n8
TELRA TELETEXT

PCF84C81/039 TTX-μ-Com

Pin	Name	.0	Function
1	P22	1	Link - Western/Eastern Europe
2	SDA		Serial data I^{2}C-bus
3	SCL		Serial clock I^{2}C-bus
4	P00	1	Link - select I^{2}C/MIBUS control
5	P01	1	Power Down Imminent input
6	P02	1	PL output
7	P03	1	PON output
8	P04	1	PROC data output
9	P05	1	PROC clock input
10	P06	1	MIBUS data input
11	P07	1	Data inhibit output
12	INT/T0		MIBUS DLEN, NAND, DLIM
13	T1		PL signal input
14	Vss		0C
15	XTAL 1		Crystal oscillator connection (frequency=9.830MHz ± 0.7%)
16	XTAL 2		
17	RESET		Reset circuit
18	P10	1	Link - select FASTEXT/LIST mode at Power-UP
19	P11	1	Link - ENGLISH/EUROPEAN MIBUS & screen symbols
20	P12	1	Link - 2K8/8K8 static page RAM connected
21	P13	1	Link - enable use of NVRAM
22	P14	1	Link - enable PACKET 8/30 identification display
23	P15	1	Link - enable on-screen PROGRAM prompts
24	P16	1	Link - enable LCB controlled keys/status row
25	P17	1	Link - enable STATUS ROW used in NON-FASTEXT
26	P20	1	Link - select 128/256 byte NVRAM
27	P21	1	Link - enable display of row 24
28	Vcc	1	5V(main) supply

* PCF84C81/039 option (TTX)

Pin	0	Pin LOW	Pin HIGH
1	1	E. Europe ECCT SAA5243/H	W. Europe ECCT SAA5243/E
4	1	MIBUS command input	I^{2}C command input
18	1	LIST mode at power-up	FASTEXT mode at power-up
19	1	European MIBUS & symbols	English MIBUS & symbols
20	1	2K8 static RAM connected	8K8 static RAM connected
21	1	No NVRAM connected	Enable use of NVRAM
22	1	Disable 8/30 display	Enable 8/30 display
23	1	Disable on-screen prompts	Enable on-screen prompts
24	1	Disable LCB decoding	Enable LCB decoding
25	1	Disable row 24 if no x/27	Enable row 24 if no x/27
26	1	256 x 8 NVRAM connected	128 x 8 NVRAM connected
27	1	Disable display of row 24	Enable display of row 24

I-F CIRCUIT

TDA8340;Q
TDA8341;Q

TELEVISION IF AMPLIFIER AND DEMODULATOR

The TDA8340;Q and TDA8341;Q are integrated IF amplifier and demodulator circuits for colour or black/white television receivers, the TDA8340;Q is for application with n-p-n tuners and the TDA8341;Q for p-n-p tuners.

The TDA8340;Q and TDA8341;Q are pin-compatible successors with improved performance to types TDA2540/2541;Q and TDA3540/3541;Q.

Features

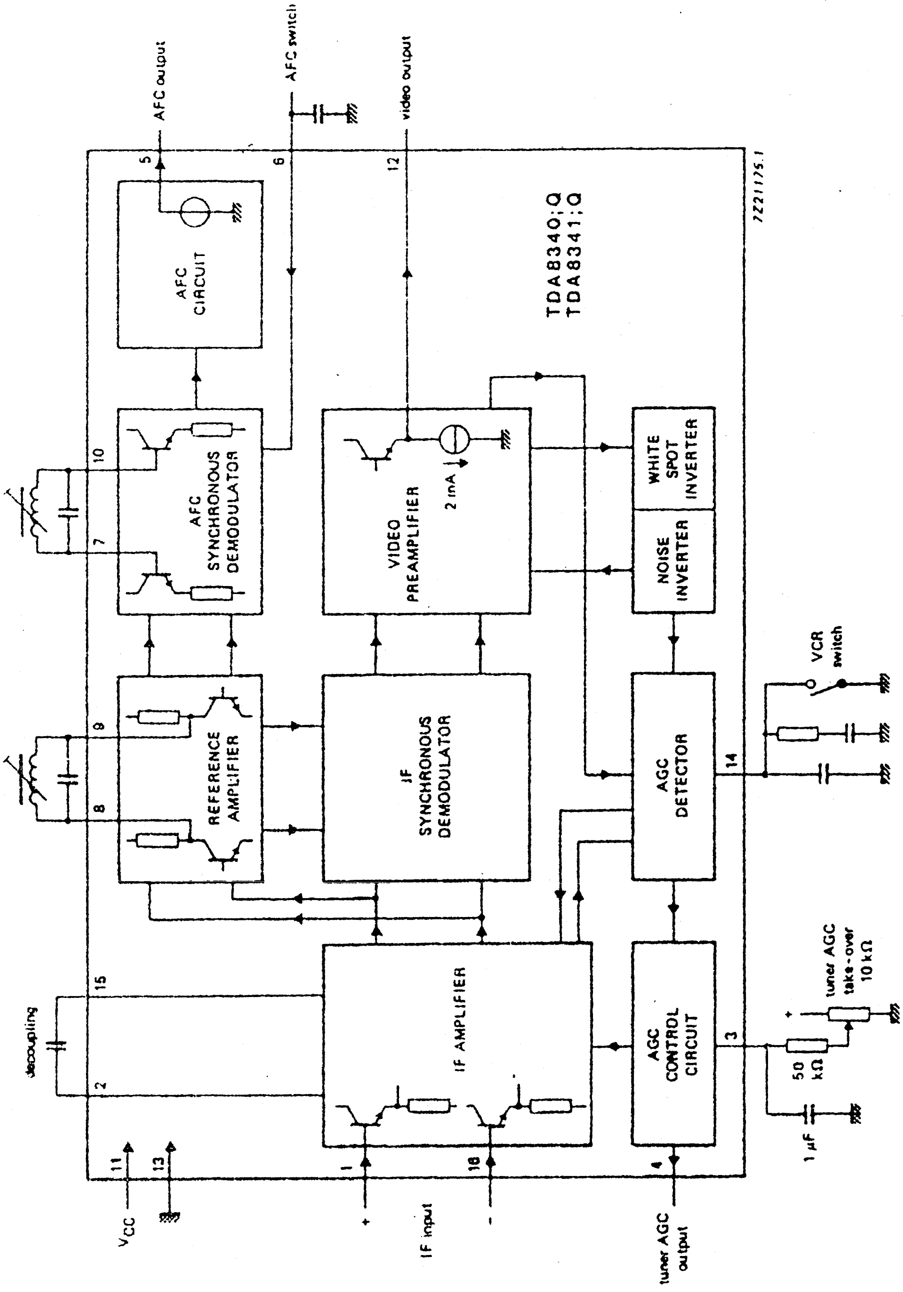
- Full range gain-controlled wide-band IF amplifier
- Linear synchronous demodulator with excellent intermodulation performance
- White spot inverter
- Wide-band video amplifier with noise protection
- AFC circuit with AFC on/off switching and sample-and-hold function
- Low impedance AFC output
- AGC circuit with noise gating
- Tuner AGC output for n-p-n tuners (TDA8340) or p-n-p tuners (TDA8341)
- External video switch for switching-off the video output
- Reduced sensitivity for high sound carriers
- Integrated filter to limit second harmonic IF signals
- Wide supply voltage range
- Requires few external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11\text{-}13}$	9,4	12	13,2	V
Supply current (pin 11)		I_{11}	30	42	55	mA
IF input sensitivity (r.m.s. value)		$V_{1\text{-}16(rms)}$	20	40	80	µV
IF gain control range		G_v	–	67	–	dB
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12\text{-}13(p\text{-}p)}$	2,4	2,7	3,0	V
Signal-to-noise ratio	V_i = 10 mV	S/(S+N)	50	58	–	dB
AFC output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	--	V

PACKAGE OUTLINES

TDA8340; TDA8341: 16-lead DIL; plastic (SOT38).
TDA8340Q; TDA8341Q: 16-lead QIL; plastic (SOT58).


AFC output
AFC switch
video output
5
6
12
AFC CIRCUIT
TDA8340;Q
TDA8341;Q
7Z21175.1
AFC SYNCHRONOUS DEMODULATOR
10
7
VIDEO PREAMPLIFIER
2 mA
WHITE SPOT INVERTER
NOISE INVERTER
REFERENCE AMPLIFIER
9
8
IF SYNCHRONOUS DEMODULATOR
AGC DETECTOR
14
VCR switch
IF AMPLIFIER
15
2
decoupling
AGC CONTROL CIRCUIT
3
tuner AGC take-over 10 kΩ
50 kΩ
1 µF
11
13
VCC
1
18
+
IF input
−
4
tuner AGC output

PINNING

1 and 16	Balanced IF inputs
2 and 15	IF amplifier decoupling
3	Tuner AGC starting point adjustment
4	Tuner AGC output
5	AFC output
6	AFC on/off switch and sample-and-hold capacitor
7 and 10	Reference carrier π/2 rad. phase shift
8 and 9	IF picture carrier passive regeneration
11	Positive supply voltage (V_{CC})
12	Video output
13	Ground (V_{EE})
14	IF AGC capacitor and VCR switch

FUNCTIONAL DESCRIPTION

IF amplifier

This is a 3-stage, gain-controlled IF amplifier with a wide dynamic range. On-chip capacitors in the d.c. feedback loop of the amplifier maintain stability at maximum gain. Internal stabilization of the supply voltage ensures the desired sensitivity and gain control range over the whole supply voltage range and also gives very good power supply ripple rejection in this part of the circuit.

Demodulator

The redesigned IF demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and logarithmic clamping to give improved signal handling. The demodulator input is a.c. coupled to the IF amplifier to reduce d.c. offsets and thus minimize residual IF carrier in the output signal.

Video amplifier

The linearity and bandwith of the video amplifier are sufficient to meet all wide band requirements, e.g. for teletext transmissions. Second harmonics of the IF carrier are effectively reduced by a Sallen-Key low pass interstage filter between the demodulator output and the video amplifier input. An integrated filter in the noise inverter reduces the sensitivity of the video amplifier for high sound carriers.

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers.

Note. To prevent radiated video output at the input pins, connect a 6,8 μH inductor in series with pin 12 and fit as close as possible to the IC body. Use short leads.

AGC dectector

A Bessel low-pass filter between the video output and the AGC detector improves the detector function in the presence of high sound carriers. No 'hang-up' occurs in the detector after pin 14 has been short-circuited to ground (VCR switch operated). The detector also generates the sample-and-hold pulse for the AFC system.

AGC control circuit

This converts the AGC detector voltage (pin 14) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted via pin 3.

CHARACTERISTICS

Measured in circuit of Fig. 3; $V_{CC} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current	no input signal	I_{11}	30	42	55	mA
IF amplifier (note 1)						
Input sensitivity	at onset of AGC	V_{1-16}	20	40	80	µV
Differential input resistance		R_{1-16}	–	2	–	kΩ
Differential input capacitance		C_{1-16}	–	3	–	pF
Gain control range		G_v	–	67	–	dB
Input signal variation	note 2	V_{12-13}	–	–	0,5	dB
Maximum input signal		V_{1-16}	100	–	–	mV
Tuner AGC (note 1)						
Tuner AGC starting point	$R_{3-11} = 39$ kΩ	V_{1-16}	–	–	3	mV
(note 3)	$R_{3-13} = 39$ kΩ	V_{1-16}	70	–	–	mV
Maximum current swing of tuner AGC output		I_4	10	–	–	mA
Input signal variation	note 4; $I_4 = 1$ to 9 mA	V_{1-16}	–	–	3	dB
Output saturation voltage	$I_4 = 7$ mA	V_{4-13}	–	200	300	mV
Leakage current	$V_4 = 12$ V	I_4	–	–	1	µA
Video output (note 4)						
Zero-signal output level	note 5	V_{12-13}	5,7	6,0	6,3	V
Top sync output level		V_{12-13}	2,8	3,0	3,2	V
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Internal bias current of emitter follower output transistor			1,4	2,2	3,0	mA
Output impedance		Z_{12}	–	100	–	Ω
Bandwith of demodulated output signal		B	6	7,5	–	MHz
Differential gain	note 6	G_d	–	2	5	%
Differential phase	note 6	φ_d	–	2	5	deg
Luminance non-linearity	note 7		–	2	5	%
Residual carrier signal (r.m.s. value)	note 8	$V_{12-13(rms)}$	–	2	10	mV

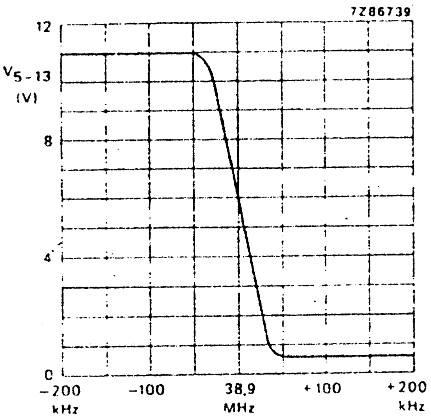


Fig. 2 AFC output voltage as a function of frequency.

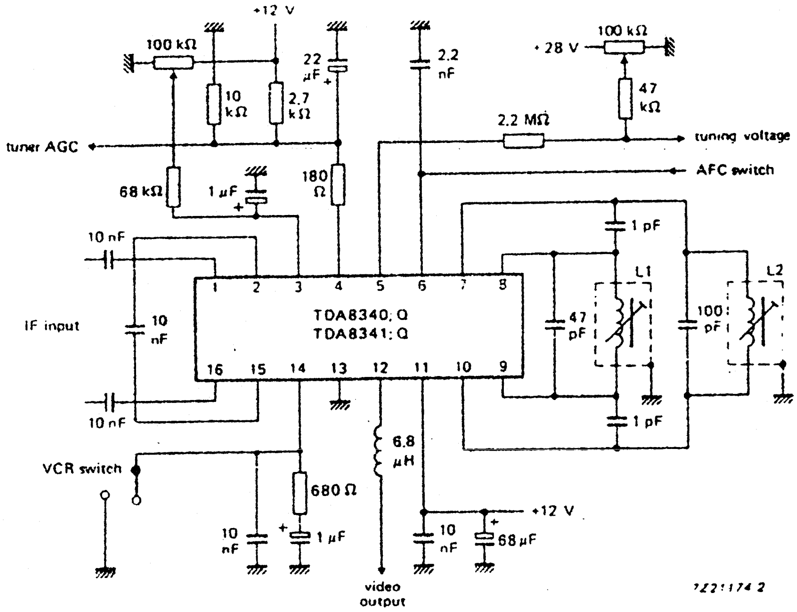

+12 V
100 kΩ
22 µF
2.2 nF
100 kΩ
+28 V
10 kΩ
2,7 kΩ
47 kΩ
2,2 MΩ
tuner AGC
tuning voltage
AFC switch
68 kΩ
1 µF
180 Ω
10 nF
1 pF
L1
L2
IF input
10 nF
TDA8340; Q
TDA8341; Q
47 pF
100 pF
1 2 3 4 5 6 7 8
16 15 14 13 12 11 10 9
10 nF
1 pF
VCR switch
6,8 µH
680 Ω
+12 V
10 nF
1 µF
10 nF
68 µF
video output
7Z21174 2

Fig. 3 Typical application circuit diagram;
Q of L1 and L2 = 80; f_0 = 38,9 MHz.

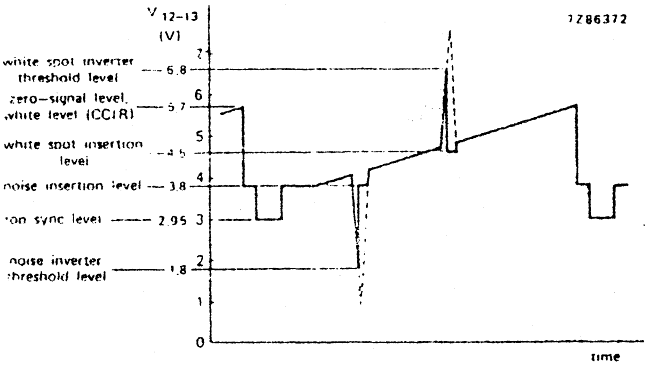


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

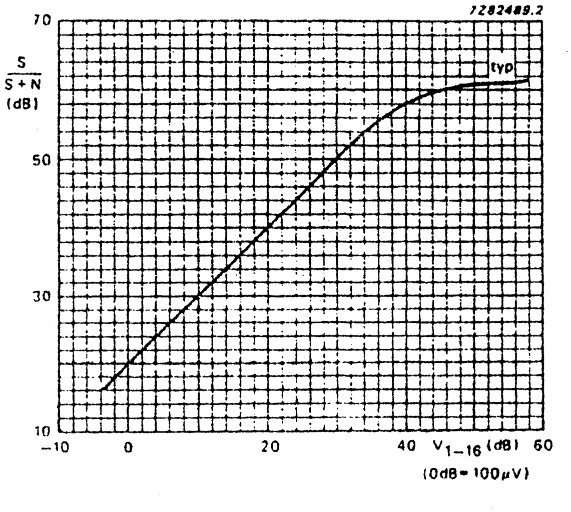
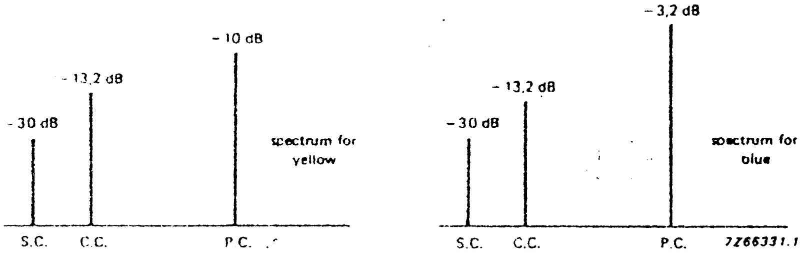


Fig. 5 Signal-to-noise ratio as a function of input voltage.



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level

with respect to top sync level

Fig. 6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

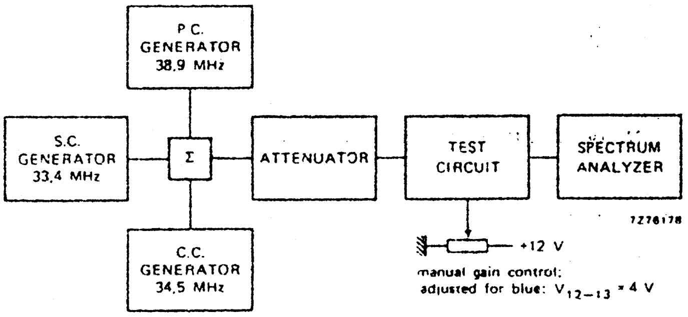

P.C. GENERATOR 38,9 MHz
S.C. GENERATOR 33,4 MHz
Σ
C.C. GENERATOR 34,5 MHz
ATTENUATOR
TEST CIRCUIT
SPECTRUM ANALYZER
7Z78178
+12 V
manual gain control; adjusted for blue: $V_{12-13} = 4$ V

Fig. 7 Test set-up for intermodulation measurements.

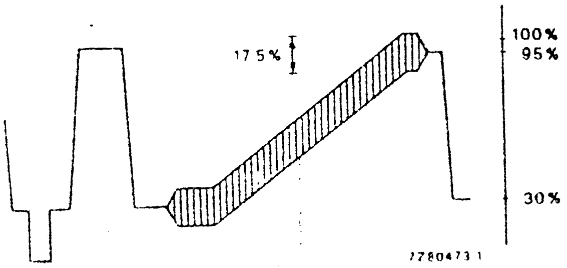


Fig. 8 Video output signal.

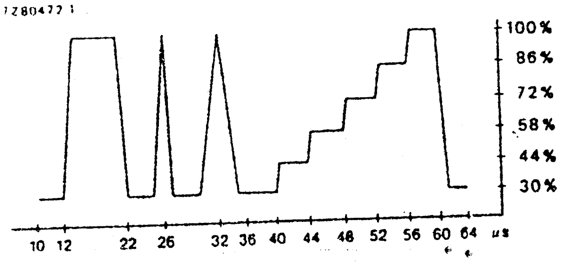


Fig. 9 E.B.U. test signal waveform (line 330).

FUNCTIONAL DESCRIPTION (continued)

AFC circuit

The AFC circuit provides a voltage output which controls the IF frequency of the tuner. Video information on the AFC output (pin 5) is eliminated by a sample-and-hold circuit (external capacitor at pin 6). Coupling between the AFC and reference tuned circuits is via two small capacitors (or parasitic capacitance) between the respective tracks of the printed circuit board. If the capacitance is less than 1 pF, the steepness of the AFC characteristic is reduced.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 11)	$V_{CC} = V_{11\text{-}13}$	9,4	13,2	V
IF AGC voltage/VCR switch	$V_{14\text{-}13}$	–	13,2	V
Tuner AGC voltage	$V_{4\text{-}13}$	–	12	V
AFC switch voltage	$V_{6\text{-}13}$	–	13,2	V
Maximum voltage level with VCR switch active	$V_{12\text{-}13}$	–	5,0	V
DC current at video output	I_{12}	–	10	mA
DC current at AFC output	I_5	–	10	mA
Total power dissipation	P_{tot}	–	1,2	W
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature	T_{amb}	–25	+70	°C

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA3827
TV-sound demodulator circuit with SCART switches and AF control

FEATURES

- Wide supply voltage range from 4.5 V to 13.2 V
- Wide frequency range from 4 to 12 MHz
- High ripple rejection
- High precision and temperature compensated FM-demodulator output
- Multiple-input AF operational amplifiers with offset compensation
- SCART AF input / AF output (low impedance)
- External AF input
- High-level AF output voltage with low distortion
- External selection of the source selector AF gain
- Low switching noise between AF and mute
- Wide volume-control range

GENERAL DESCRIPTION

The TDA3827 contains a single FM demodulator with SCART switches, a mute function and volume control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	$V_P = 5$ V	–	26	–	mA
		$V_P = 12$ V	–	28	–	mA
(S+N)/N	signal to weighted noise		73	78	–	dB
$V_{5(rms)}$	FM demodulator output voltage (RMS value)	$\Delta f = 50$ kHz; $f_{mod} = 1$ kHz; $Q_L = 20$	450	500	550	mV
$V_{13(rms)}$	SCART output signal (RMS value)		–	1.0	–	V
G_v	volume control range		80	85	–	dB
$V_{17(rms)}$	AF output signal (RMS value)	$\Delta f = 50$ kHz; $f_{mod} = 1$ kHz; $Q_L = 20$	–	1.0	–	V
THD	total harmonic distortion (pin 17)		–	0.5	–	%

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3827	18	DIL	plastic	SOT102

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

PIN CONFIGURATION

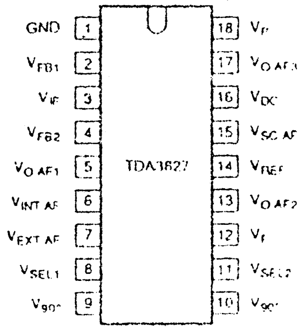

GND 1
V_FB1 2
V_IF 3
V_FB2 4
V_O AF1 5
V_INT AF 6
V_EXT AF 7
V_SEL1 8
V_90° 9
TDA3827
18 V_P
17 V_O AF3
16 V_DC
15 V_SC AF
14 V_REF
13 V_O AF2
12 V_F
11 V_SEL2
10 V_90°

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{FB1}	2	limiter amplifier feedback
V_{IF}	3	FM IF input signal
V_{FB2}	4	limiter amplifier feedback
$V_{O\,AF1}$	5	AF output signal
$V_{INT\,AF}$	6	internal AF input signal
$V_{EXT\,AF}$	7	external AF input signal
V_{SEL1}	8	selection voltage for internal / external AF input and mute
$V_{90°}$	9	quadrature demodulator tuned circuit reference
$V_{90°}$	10	
V_{SEL2}	11	selection voltage for internal / external or SCART audio
V_F	12	source selector feedback
$V_{O\,AF2}$	13	output signal to SCART
V_{REF}	14	reference voltage
$V_{SC\,AF}$	15	input signal from SCART
V_{DC}	16	DC volume control voltage
$V_{O\,AF3}$	17	AF output signal from volume control
V_P	18	supply voltage

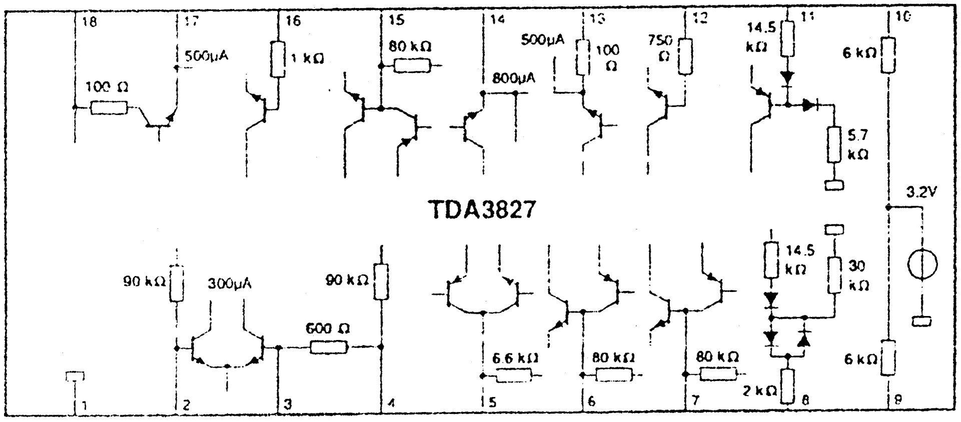

18
17
16
15
14
13
12
11
10
100 Ω
500µA
1 kΩ
80 kΩ
500µA
800µA
100 Ω
750 Ω
14.5 kΩ
6 kΩ
5.7 kΩ
3.2V
TDA3827
90 kΩ
300µA
90 kΩ
600 Ω
6.6 kΩ
80 kΩ
80 kΩ
14.5 kΩ
30 kΩ
2 kΩ
6 kΩ
1
2
3
4
5
6
7
8
9

Fig.3 Internal circuits.

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source selector control (see Fig.5)						
V_8	voltage for internal selection of AF-input (pin 6)		$1/3\ V_P$	–	$2/3\ V_P$ -0.7	V
I_8	selection input current		–	–	200	µA
V_8	voltage for external selection of AF-input (pin 7)		$2/3\ V_P$ $+0.7$	–	V_P	V
I_8	selection input current		40	–	600	µA
V_8	voltage for mute active		0	–	$1/3\ V_P - 1$	V
I_8	input current		−10	–	−500	µA
SCART switch and level control						
$V_{15(rms)}$	AC input signal (RMS value)		–	500	1000	mV
Z_{15}	input impedance		50	80	–	kΩ
$G_{17\text{-}15}$	voltage gain	$V_{16} = 4.1$ V	−1.5	0	+1.5	dB
G_{max}	maximum voltage gain	$V_{16} = 5.0$ V	+4.0	+5.0	+6.0	dB
ΔG_V	volume control range	see Fig.7	80	86	–	dB
V_{17}	DC voltage		–	2.3	–	V
I_{17}	DC output current		–	–	−1	mA
Z_{17}	dynamic output impedance		–	–	10	Ω
C_L	capacitive output load (pin 17)		–	–	1500	pF
$V_{17(rms)}$	output signal (RMS value)	THD ≤ 1 %	–	1.0	1.1	V
	noise voltage (RMS value)	$B_{noise} = 20$ kHz	–	100	–	µV
B_{AF3}	small signal bandwidth (pin 17)	at −3 dB	50	100	–	kHz
THD	distortion (pin 17)	at maximum gain	–	0.5	1.0	%
ΔV_{17}	offset voltage between internal and SCART		–	5	20	mV
V_{16}	control voltage	minimum gain −80 dB; see Fig.7	0.7	1.0	–	V
I_{16}	control current		–	–	50	µA
$\alpha_{6,7/15}$	crosstalk attenuation between IF-stage and control-stage	IF sound modulated; SCART switch on; source-selector on position input 1	80	90	–	dB
SCART switch control (see Fig.6)						
V_{11}	voltage for internal active		0	–	$4/5\ V_P - 3$	V
I_{11}	current		0	–	−100	µA
V_{11}	voltage for SCART active		$4/5\ V_P - 1$	–	13.2	V
I_{11}	current		$\frac{V_{11} - 1.4}{20.000}$	–	700	µA

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

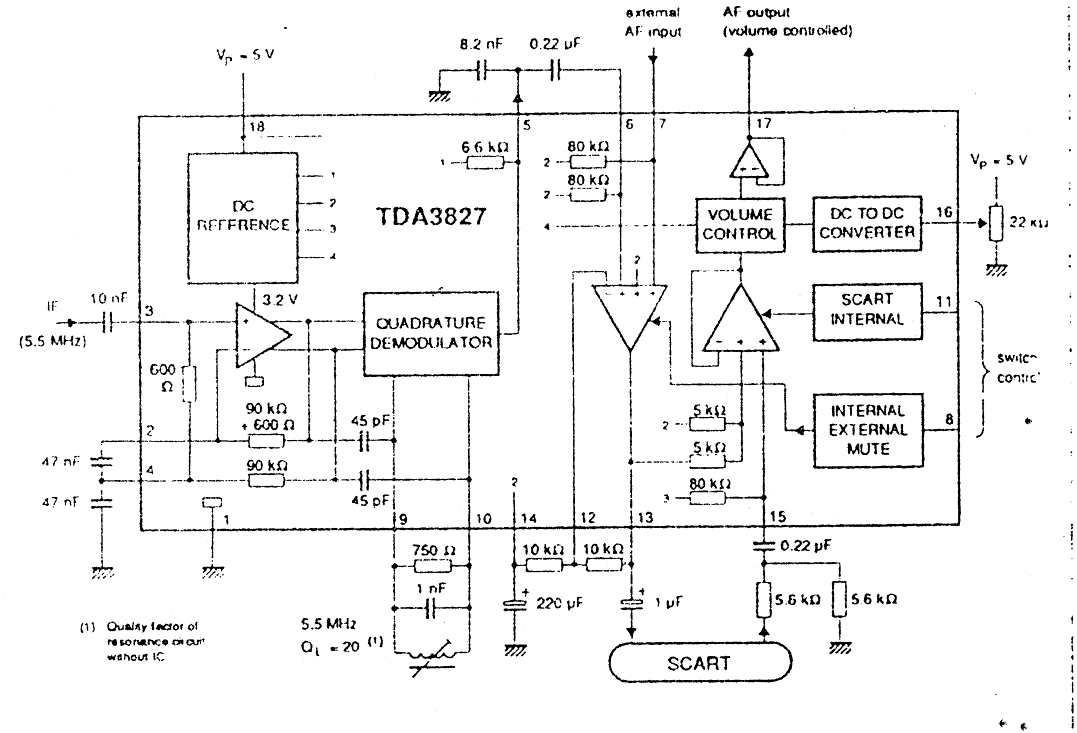

external AF input
AF output (volume controlled)
V_P = 5 V
8.2 nF
0.22 µF
18
5
6
7
17
6.6 kΩ
80 kΩ
80 kΩ
DC REFERENCE
TDA3827
VOLUME CONTROL
DC TO DC CONVERTER
16
22 kΩ
IF (5.5 MHz)
10 nF
3
3.2 V
QUADRATURE DEMODULATOR
SCART INTERNAL
11
switch control
600 Ω
90 kΩ + 600 Ω
45 pF
90 kΩ
45 pF
2
4
1
47 nF
47 nF
5 kΩ
5 kΩ
80 kΩ
INTERNAL EXTERNAL MUTE
8
9
10
14
12
13
15
750 Ω
1 nF
10 kΩ
10 kΩ
220 µF
1 µF
0.22 µF
5.6 kΩ
5.6 kΩ
5.5 MHz
Q_L = 20 (1)
SCART
(1) Quality factor of resonance circuit without IC.

Fig.1 Block diagram.

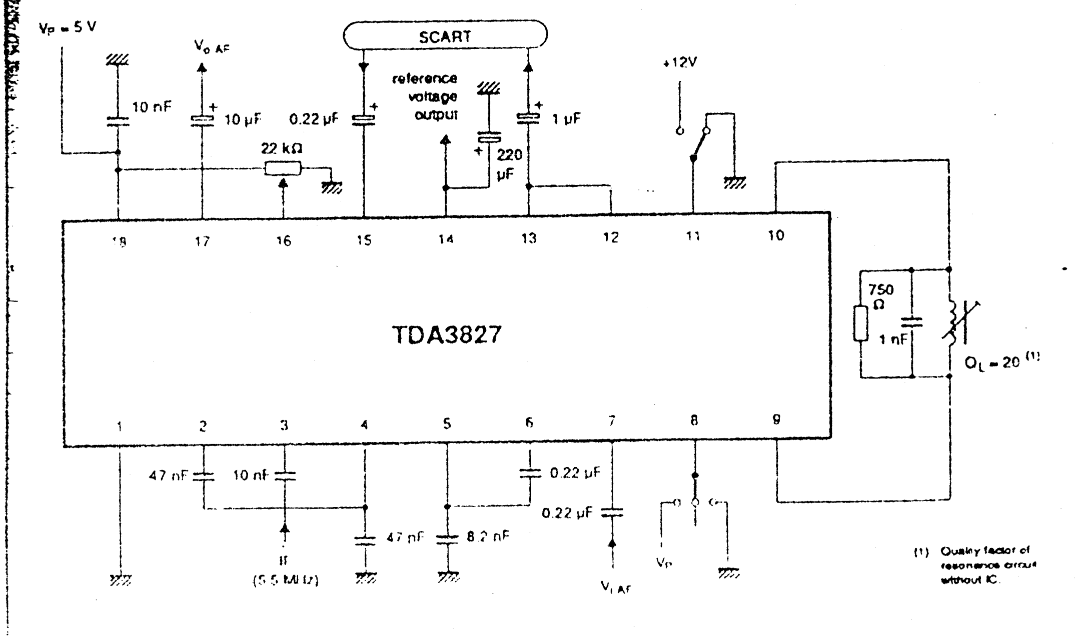

V_P = 5 V
$V_{o\,AF}$
SCART
reference voltage output
+12V
10 nF
10 µF
0.22 µF
22 kΩ
220 µF
1 µF
18
17
16
15
14
13
12
11
10
TDA3827
1
2
3
4
5
6
7
8
9
750 Ω
1 nF
Q_L = 20 (1)
47 nF
10 nF
47 nF
8.2 nF
0.22 µF
0.22 µF
IF (5.5 MHz)
V_P
$V_{i\,AF}$
(1) Quality factor of resonance circuit without IC.

Fig.2 Test circuit.

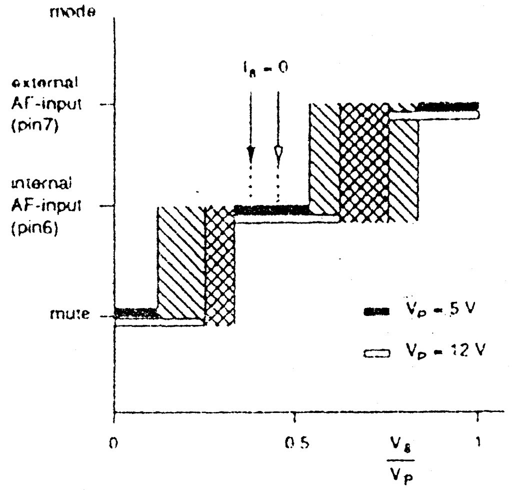


Fig.5 Source selector switching levels.

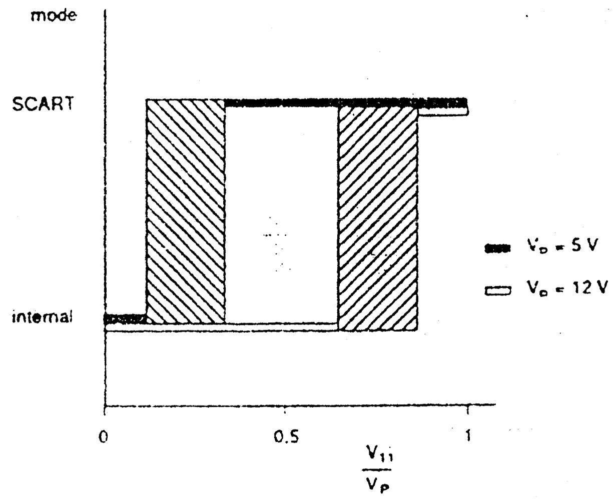


Fig.6 SCART switching levels.

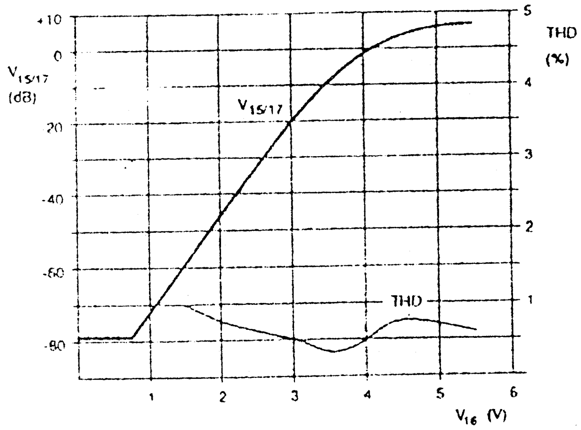


Fig.7 Volume control diagram.

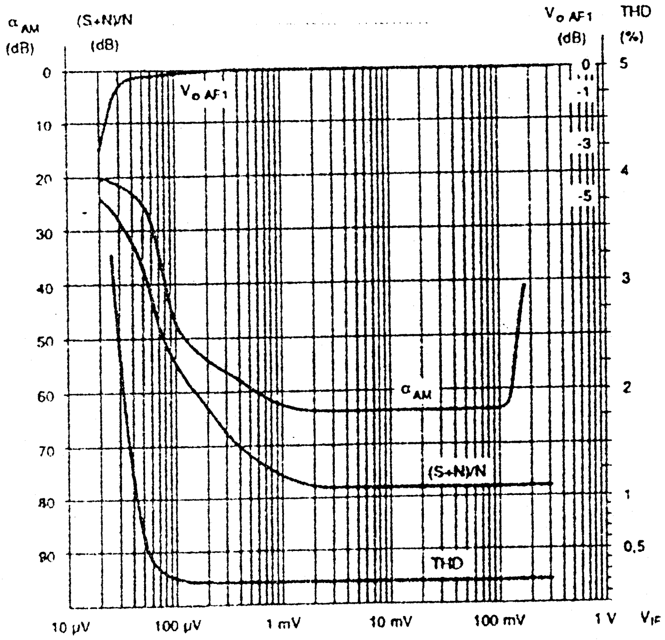


Fig.8 AF output voltage at pin 5, THD, (S+N)/N in accordance with to CCIR468-3 and AM suppression α_{AM} as functions of IF input voltage V_{IF} at pin 3.

SECAM CIRCUIT

TDA3592A

SECAM-PAL TRANSCODER

GENERAL DESCRIPTION

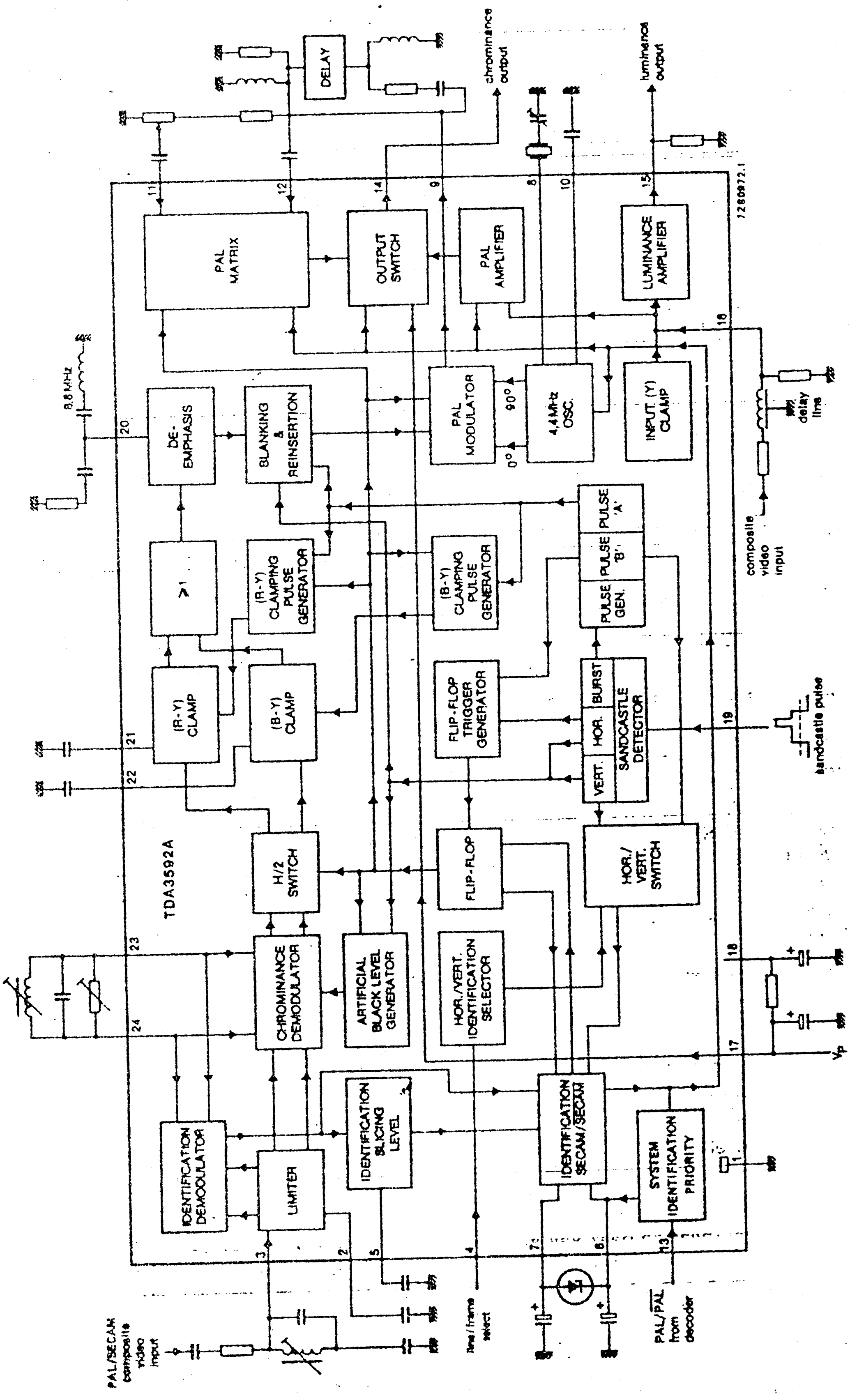
The TDA3592A transcoder circuit converts SECAM input signals into true PAL signals, and can be used in combination with all types of PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to provide true PAL signals
- 4,43 MHz oscillator
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification
- Can be used with all types of PAL decoder
- Power-saving feature operates when supply voltage falls to (typ.) 5 V: SECAM processing shuts down but $\overline{\text{SECAM}}$ signal path remains active

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	9,0	12,0	13,2	V
Supply current (pin 17)	V_P = 12 V	I_P	65	90	115	mA
Supply current (pin 17 and 18) (SECAM only)	V_P = 5 V	I_P	16	20	24	mA
Chrominance amplifier and demodulator						
Input signal $\overline{\text{SECAM}}$ (pin 3) (peak-to-peak value)		$V_{3\text{-}1(p\text{-}p)}$	–	–	1100	mV
Input signal SECAM (pin 3) (peak-to-peak value)		$V_{3\text{-}1(p\text{-}p)}$	15	100	300	mV
Output signal PAL (pin 9) (peak-to-peak value)	pin 3 = 280 kHz	$V_{9\text{-}1(p\text{-}p)}$	–	820	–	mV
Identification						
Input voltage range for horizontal identification (pin 4)		$V_{4\text{-}1}$	4,1	–	V_P	V
Input voltage range for vertical identification (pin 4)		$V_{4\text{-}1}$	0	–	2,9	V
Identification at pin 6		$V_{6\text{-}1}$	–	10,6	–	V
Slicing level reference voltage (pin 5)		$V_{5\text{-}1}$	–	7,0	–	V
Sandcastle pulse detector						
Vertical blanking level		$V_{19\text{-}1}$	–	1,5	–	V
Horizontal blanking level		$V_{19\text{-}1}$	–	3,5	–	V
Burst gating level		$V_{19\text{-}1}$	–	7,0	–	V
Luminance amplifier						
Luminance input signal (peak-to-peak value)		$V_{16\text{-}1(p\text{-}p)}$	–	1,2	–	V
Luminance amplifier gain at 4,4 MHz		$G_{16\text{-}15}$	–	7,0	–	dB


TDA3592A
7280972.1
DELAY
chrominance output
luminance output
PAL MATRIX
OUTPUT SWITCH
PAL AMPLIFIER
LUMINANCE AMPLIFIER
8,8 MHz
DE-EMPHASIS
BLANKING & REINSERTION
PAL MODULATOR
0°
90°
4,4 MHz OSC.
INPUT (Y) CLAMP
delay line
composite video input
>1
(R-Y) CLAMPING PULSE GENERATOR
(B-Y) CLAMPING PULSE GENERATOR
PULSE 'A'
PULSE 'B'
PULSE GEN.
(R-Y) CLAMP
(B-Y) CLAMP
FLIP-FLOP TRIGGER GENERATOR
VERT.
HOR.
BURST
SANDCASTLE DETECTOR
sandcastle pulse
H/2 SWITCH
FLIP-FLOP
HOR./VERT. SWITCH
CHROMINANCE DEMODULATOR
ARTIFICIAL BLACK LEVEL GENERATOR
HOR./VERT. IDENTIFICATION SELECTOR
IDENTIFICATION DEMODULATOR
LIMITER
IDENTIFICATION SLICING LEVEL
IDENTIFICATION SECAM/SECAM
SYSTEM IDENTIFICATION PRIORITY
PAL/SECAM composite video input
line/frame select
PAL/PAL from decoder
Vp
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3592A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or $\overline{\text{SECAM}}$ (NTSC, PAL or black-and-white).

When the incoming signals are PAL they are diverted via pin 16 to the chrominance output at pin 14 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM-PAL transcoding process. When SECAM signals are received, the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 3 via an external bell filter. The signals are amplified, limited and then demodulated. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same DC level. With all conditions at pin 4, artificial black levels are inserted during the horizonta blanking periods. This is done because of the possibility of horizontal burst signals not being availabl The artificial levels may not be identical to the detected black level due to circuit spread but this can be corrected by detuning the reference tuned circuit.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits. The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the PAL modulator. At this input the phase relationship for magenta colour is +(R-Y) and −(B-Y). The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; for a magenta colour the modulated (R-Y) component has the same phase position as the (R-Y) burst. The (B-Y) burst is modulated 180° out o phase with respect to the (B-Y) component of a magenta-coloured input signal.

Identification SECAM/$\overline{\text{SECAM}}$

Identification of the SECAM signal is performed using the fact that only SECAM signals have a line-to-line difference in voltage level. The identification circuit compares the phase of the demodulated voltage difference waveform with the phase of the flip-flop output. If the phase relationship is not correct, the flip-flop is reset by an extra pulse from the flip-flop trigger generator. For horizontal identification the phase comparison is performed during the period of pulse 'B' (see Fig. 2). When vertical identification is selected, the comparison is performed only during the horizontal scan of the vertical blanking. The SECAM identification circuits operate when selected by the voltage on pin 4; this may be horizontal, vertical or combined horizontal and vertical identificatio depending on the switching arrangements of pin 4.
These are as follows:

- Horizontal identification preset when $V_{4-1} < 2{,}9$ V;
- Vertical identification preset when $V_{4-1} > 4{,}1$ V;
- Horizontal/vertical combination when sandcastle pulse is present on pin 4.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detector burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL modulator burst and to sample the (R-Y) and (B-Y) clamping pulse generators. A (R-Y) clamping pulse is generated only during a red line and a (B-Y) clamping pulse only during a blue line. Pulse 'B' times the SECAM horizontal identification.

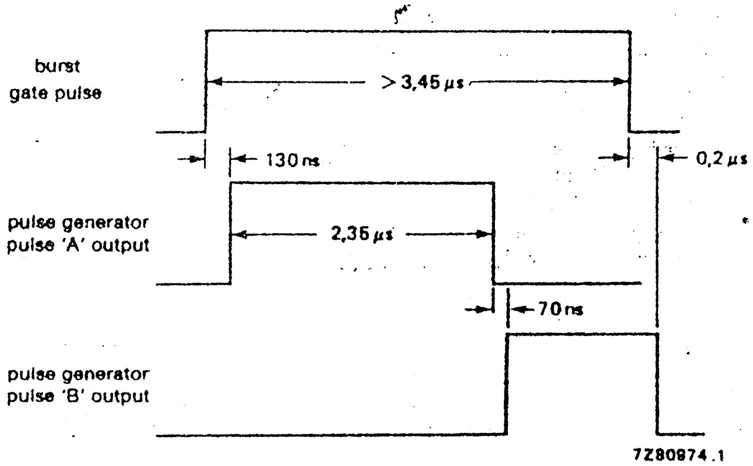

burst gate pulse
> 3,45 μs
130 ns
0,2 μs
pulse generator pulse 'A' output
2,36 μs
70 ns
pulse generator pulse 'B' output
7Z80974.1

Fig. 2 Burst gate timing pulse generation.

Carrier generation

The carrier signal for the PAL modulator is obtained from a 4,43 MHz oscillator. An internal Miller integrator operates in conjunction with the decoupling capacitor at pin 10 to provide the required 90° phase shift.

PAL matrix

The signal output from the PAL modulator at pin 9 is sequentially modulated with (R-Y) burst phased in the +(R-Y) direction, and (B-Y) burst phased in the −(B-Y) direction. This PAL signal is applied directly to pin 11 and via a 64 μs delay to pin 12. A true PAL signal is constructed in the PAL matrix by means of an additional/substraction process (in a correct H/2 sequence) using the delayed and undelayed inputs.

FUNCTIONAL DESCRIPTION (continued)

Coupling of identification systems

Coupling of a TDA3592A and a PAL decoder can be performed to obtain an optimum identification system. The system operates using the functions of pins 13, 6 and 7: the voltage level at pin 13 is controlled by the PAL/$\overline{\text{PAL}}$ detection of the PAL decoder; and the voltage level at pins 6 and 7 are functions of SECAM/$\overline{\text{SECAM}}$ detection in the TDA3592A.

The circuit action is as follows and is summarized in Table 1.

Channel switching	During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V), this corresponds to the $\overline{\text{SECAM}}$ mode of the TDA3592A.
PAL	The high voltage level at pin 6 caused by channel switching is maintained by the TDA3592A when it recognizes the signal as $\overline{\text{SECAM}}$ (this condition is maintained even if reflected PAL signals are present). The PAL decoder recognizes the signal as PAL and takes pin 13 of TDA3592A to a voltage greater than 1,7 V. The TDA3592A is now held in the $\overline{\text{SECAM}}$ condition by an internal current source at pin 6.
SECAM	The initial high voltage level (+ 10,2 V) at pin 6 caused by channel switching sets the TDA3592A in the $\overline{\text{SECAM}}$ mode and during this time the PAL decoder detects a $\overline{\text{PAL}}$ signal. This causes a voltage at pin 13 of < 1,1 V which prevents the internal current source of TDA3592A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3592A to detect SECAM. The initiation of SECAM detection is delayed by the action of the external circuit at pins 6 and 7 and commences as pin 6 approaches 7,0 V. The SECAM signals are converted by TDA3592A to PAL signals at pin 14, which results in the PAL decoder switching to the PAL mode (the TDA3592A remains in the SECAM mode).
Black-and-white	The TDA3592A is initially set in the $\overline{\text{SECAM}}$ mode as previously described. The PAL decoder detects $\overline{\text{PAL}}$ and the TDA3592A detects $\overline{\text{SECAM}}$ which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3592A	PAL decoder mode	System operating mode
SECAM	PAL	SECAM
SECAM	$\overline{\text{PAL}}$	condition not used
$\overline{\text{SECAM}}$	PAL	PAL
$\overline{\text{SECAM}}$	$\overline{\text{PAL}}$	black-and-white

System priorities

When TDA3592A pin 13 is connected to the PAL/$\overline{\text{PAL}}$ output of a PAL decoder, the system will give PAL priority in signal identification. Connecting TDA3592A pin 13 to ground will give SECAM priority.

Luminance and chrominance signal paths

The signal input at pin 6 is clamped by a circuit which detects the top of the luminance signal sync pulse. This clamp, the luminance signal path to pin 15 and the $\overline{\text{SECAM}}$ signal path to pin 14 remain active when the supply voltage falls to (typ.) 5 V. At this level of supply voltage the SECAM processing circuits are switched off, giving a reduction in total power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	V_P	–	13,2	V
Total power dissipation	P_{tot}	–	1,78	W
Operating ambient temperature range	T_{amb}	–25	+70	°C
Storage temperature range	T_{stg}	–25	+150	°C

CHARACTERISTICS

$V_P = V_{17\text{-}1} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.
The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1. All voltages are reference to ground pin 1.

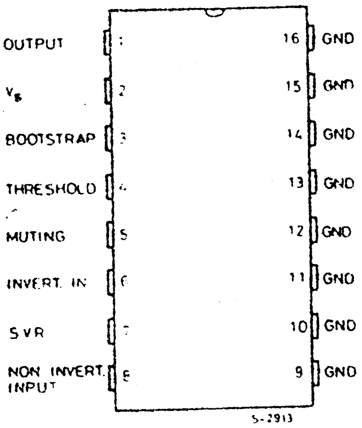
parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 17)		V_{17}	9,0	12	13,2	V
Supply current (pin 17)		I_{17}	65	90	115	mA
Supply current (pin 18)		I_{18}	40	–	160	μA
Decoupled supply voltage (pin 18)	$R_{ext17\text{-}18} = 2$ kΩ	V_{18}	8,8	11,8	13,2	V
External capacitance (pin 18)		C_{18}	–	–	10	μF
Total power dissipation		P_{tot}	–	1,08	1,38	W
Thermal resistance, junction to ambient		$R_{th\ j\text{-}a}$	–	40	45	K/W
Chrominance amplifier and demodulator						
Input signal SECAM (peak-to-peak value)		$V_{3(p\text{-}p)}$	–	–	1100	mV
Input signal SECAM at which correct limiting occurs (peak-to-peak value)		$V_{3(p\text{-}p)}$	15	100	300	mV
Input resistance (pin 3)		R_3	9,6	12,1	14,6	kΩ
Input capacitance (pin 3)		C_3	–	–	5	pF
Input resistance between pins 23 and 24		$R_{23\text{-}24}$	2,9	3,6	4,3	kΩ
Input capacitance between pins 23 and 24		$C_{23\text{-}24}$	–	12	–	pF
De-emphasis output resistance (pin 20)		R_{20}	0,9	1,1	1,3	kΩ
Chrominance demodulator zero point stability (pin 20)	note 2	f_0	–	5	–	kHz

AUDIO CIRCUIT

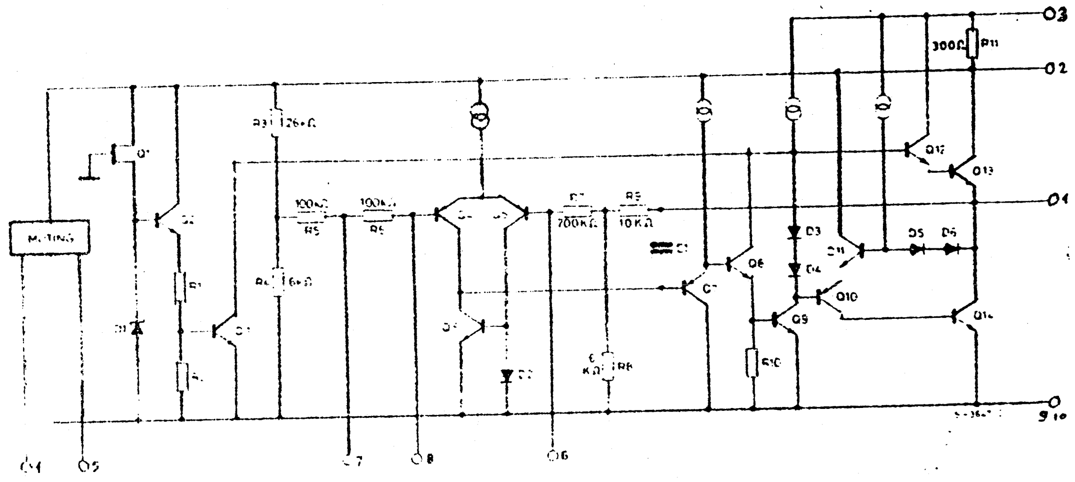
TDA1905

CONNECTION DIAGRAM

(Top view)


OUTPUT 1
V_s 2
BOOTSTRAP 3
THRESHOLD 4
MUTING 5
INVERT. IN 6
SVR 7
NON INVERT. INPUT 8
9 GND
10 GND
11 GND
12 GND
13 GND
14 GND
15 GND
16 GND
S-2913

SCHEMATIC DIAGRAM

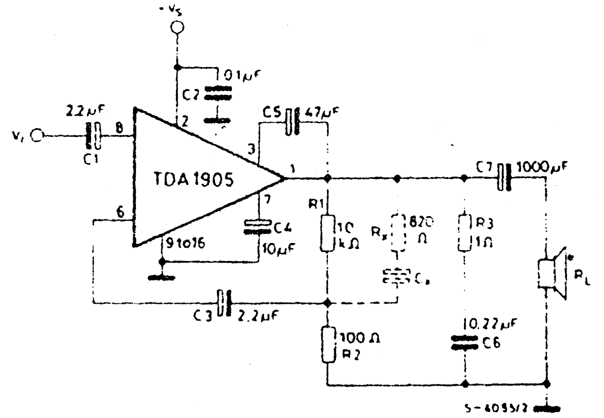

MUTING
R3 126kΩ
R4 16kΩ
100kΩ R5
100kΩ R5
R7 200kΩ
R8 10kΩ
6 kΩ R6
300Ω R11
Q12
Q13
Q14
Q10
Q9
Q6
Q7
Q11
D3
D4
D5
D6
D2
D1
R10
C1
3
2
1
9 10
4
5
7
8
6

THERMAL DATA

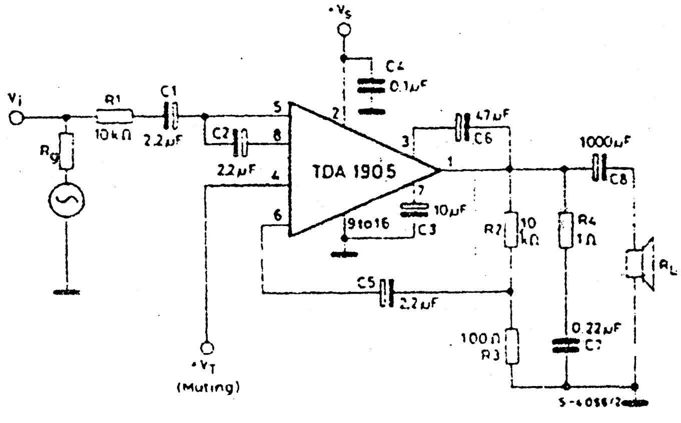
$R_{th\,j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{th\,j\text{-}amb}$	Thermal resistance junction-amb	max	70	°C/W

TEST CIRCUITS:

WITHOUT MUTING


+Vs
0.1μF
C2
2.2μF
Vi
8
2
C1
C5
47μF
3
TDA1905
1
C7
1000μF
7
R1
6
C4
10μF
9 to 16
10 kΩ
Rx
820 Ω
Cx
R3
1Ω
RL
C3
2.2μF
100 Ω
R2
0.22μF
C6
S-4055/2

WITH MUTING FUNCTION


+Vs
C4
0.1μF
Vi
R1
10kΩ
C1
2.2μF
5
2
Rg
C2
2.2μF
8
4
TDA 1905
47μF
C6
3
1
1000μF
C8
6
7
10μF
9 to 16
C3
R2
10 kΩ
R4
1Ω
RL
C5
2.2μF
100 Ω
R3
0.22μF
C7
+VT
(Muting)
S-4056/2

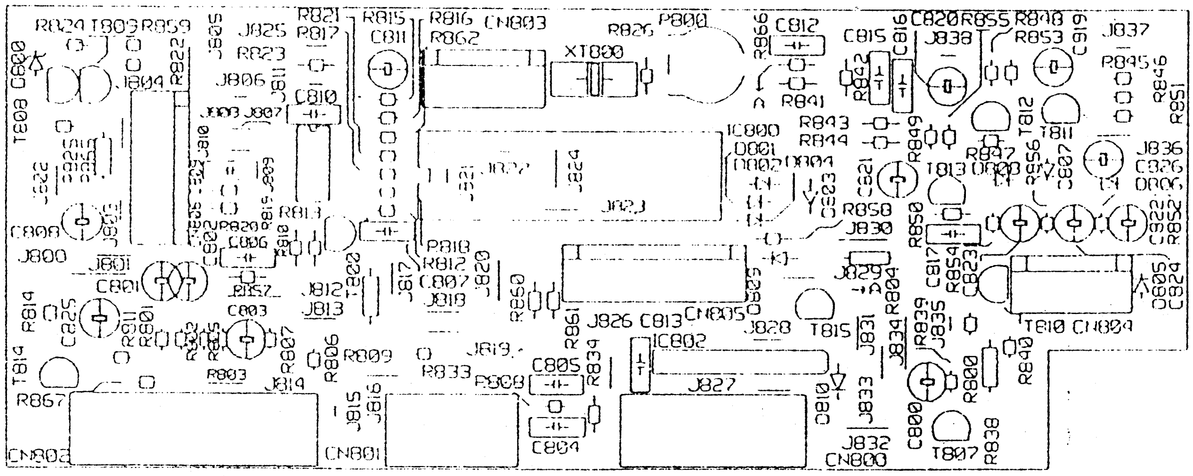
ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BW	Small signal bandwidth (-3dB)	V_s = 14V R_L = 4Ω P_o = 1W	40 to 40,000			Hz
G_v	Voltage gain (open loop)	V_s = 14V f = 1KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 14V R_L = 4Ω f = 1KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	R_g = 50Ω R_g = 1KΩ (°) R_g = 10KΩ		1.2 1.3 1.5	4.0	μV
		R_g = 50Ω R_g = 1KΩ (°°) R_g = 10KΩ		2.0 2.0 2.2	6.0	μV
S/N	Signal to noise ratio	V_s = 14V P_o = 5.5W R_L = 4Ω R_g = 10KΩ R_g = 0 (°)		90 92		dB
		R_g = 10KΩ R_g = 0 (°°)		87 87		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 8Ω f_{ripple} = 100 Hz R_g = 10KΩ V_{ripple} = 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot} = 2.5W		115		°C

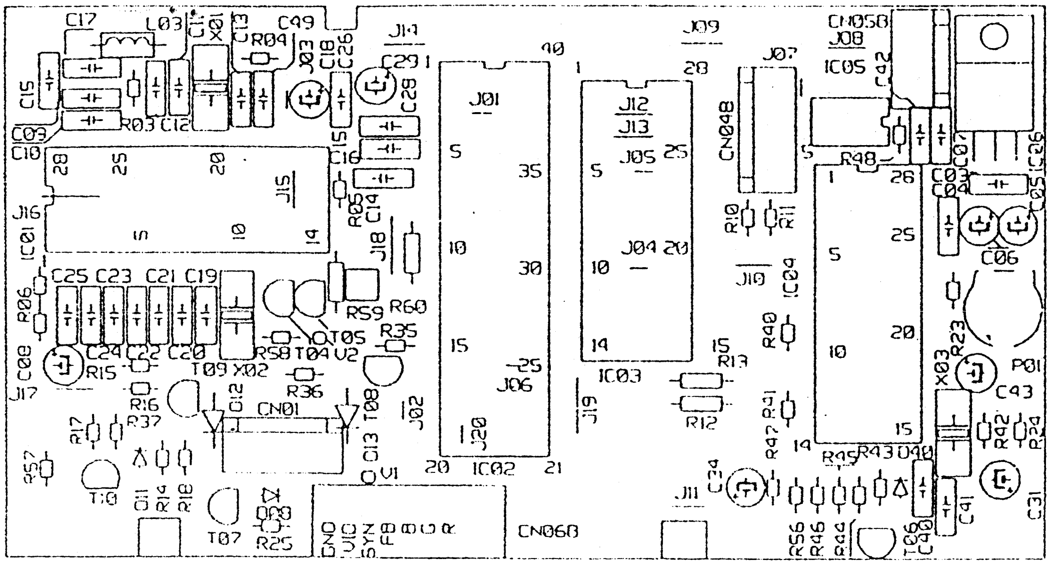
MUTING FUNCTION

V_{TOFF}	Muting-off threshold voltage (pin 4)		1.9		4.7	V
V_{TON}	Muting-on threshold voltage (pin 4)		0		1.3	V
			6.2		V_s	
R_5	Input resistance (pin 5)	Muting off	80	200		KΩ
		Muting on		10	30	Ω
R_4	Input resistance (pin 4)		150			KΩ
A_T	Muting attenuation	$R_g + R_1$ = 10KΩ	50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 30 and fig. 31



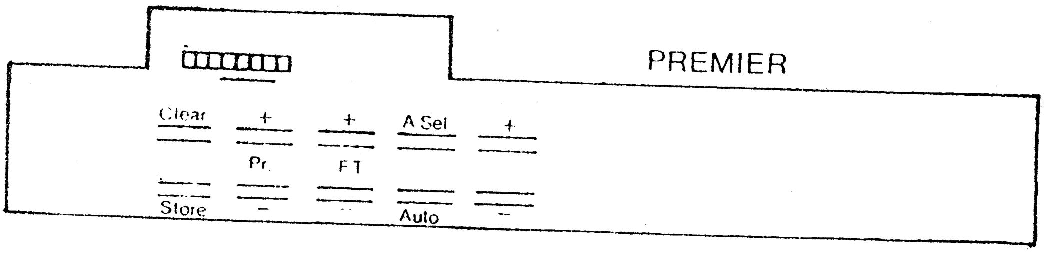
PL2 CONTROLLER BOARD



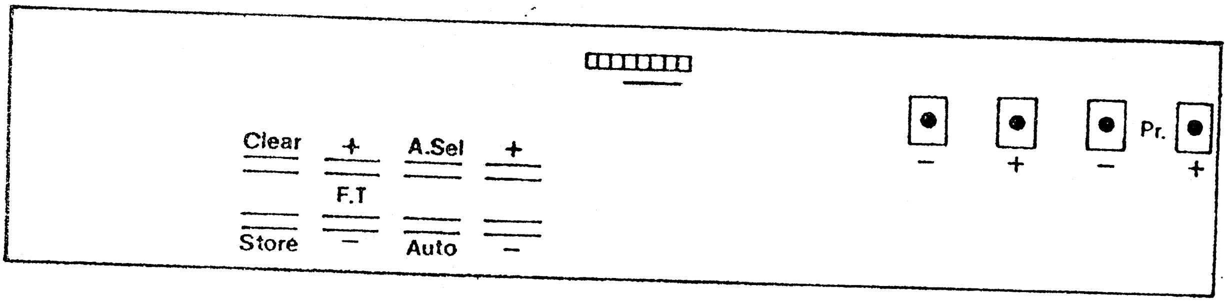
PL2 TELETEXT BOARD

TUŞ TAKIMI PCB'LERİ KEYBOARDS

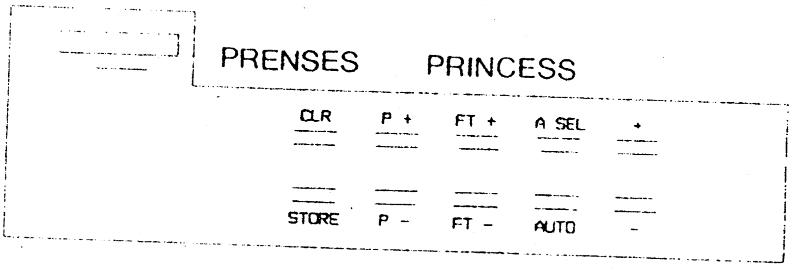
PREMIER


Clear
+
+
A Sel
+
Pr.
FT
Store
–
–
Auto
–

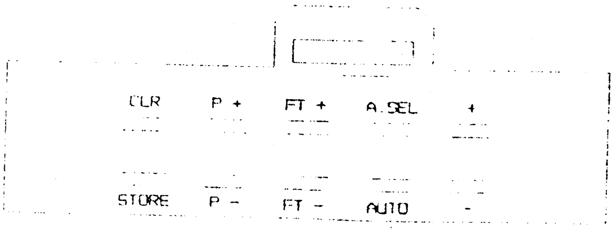
QUADRO


Clear
+
A.Sel
+
F.T
Store
–
Auto
–
–
+
–
Pr.
+

PRENSES PRINCESS

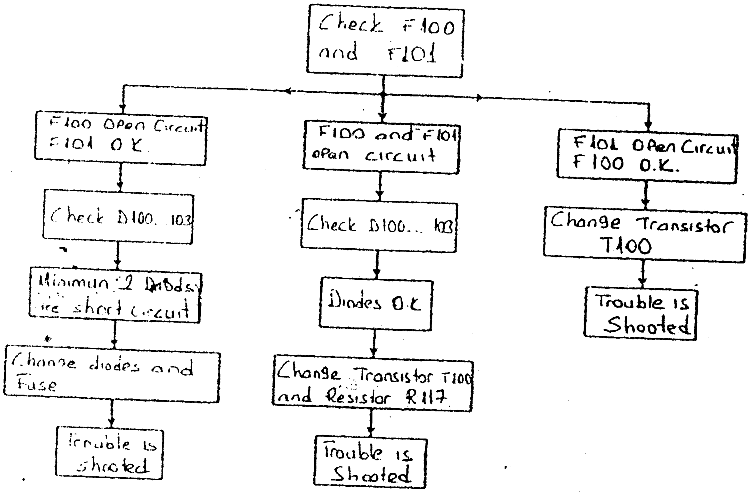

CLR
P +
FT +
A SEL
+
STORE
P –
FT –
AUTO
–

FUTURE

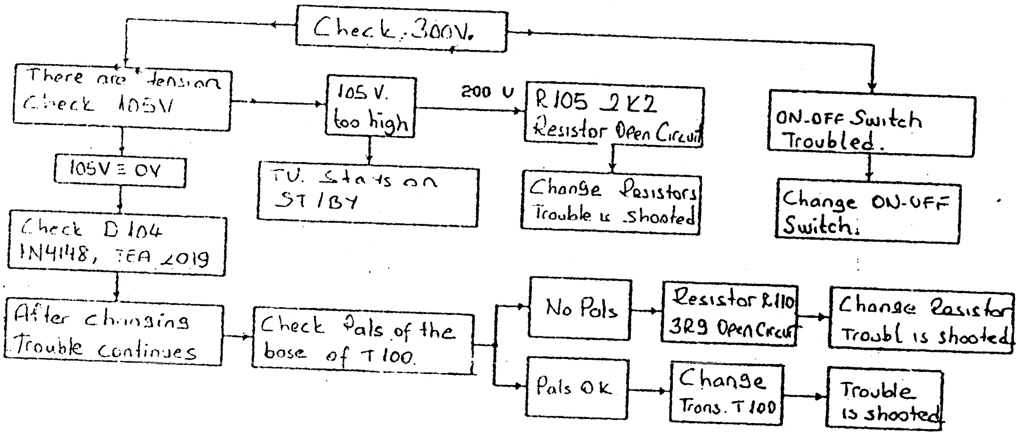

CLR
P +
FT +
A.SEL
+
STORE
P –
FT –
AUTO
–

TROUBLE SHOOTING

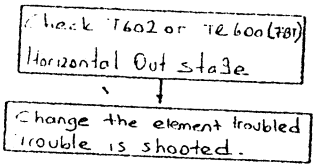
1) Dead Set (No starting signal, no Raster, no Picture, no sound)


Check F100 and F101
F100 Open Circuit F101 O.K.
F100 and F101 open circuit
F101 Open Circuit F100 O.K.
Check D100. 103
Check D100... 103
Change Transistor T100
Minimum 2 Diodes are short circuit
Diodes O.K
Trouble is Shooted
Change diodes and Fuse
Change Transistor T100 and Resistor R117
Trouble is shooted
Trouble is Shooted

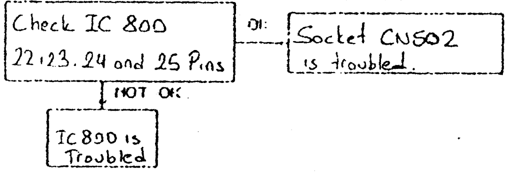
2) When Power on set doesn't start, fuses O.K.


Check 300V.
There are tension Check 105V
105 V. too high
200 V
R105 2K2 Resistor Open Circuit
ON-OFF Switch Troubled.
105V = 0V
T.V. Stays on ST/BY
Change Resistors Trouble is shooted
Change ON-OFF Switch.
Check D104 1N4148, TEA 2019
After changing Trouble continues
Check Pals of the base of T100.
No Pals
Resistor R110 3R9 Open Circuit
Change Resistor Troubl is shooted
Pals O.K
Change Trans. T100
Trouble is shooted

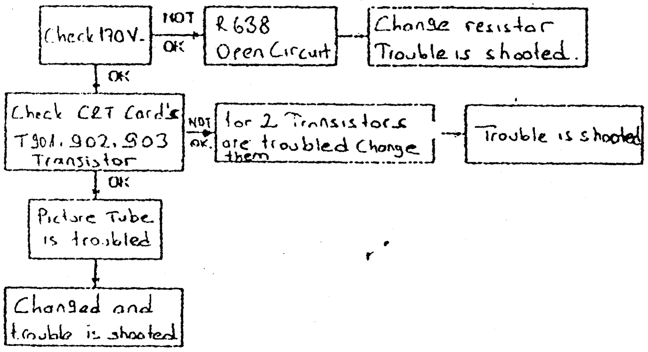
3) When Power ON 105V is about 118V Stand By led is Lighting, Sound comes from TV


Check T602 or TR600 (781) Horizontal Out stage
Change the element troubled Trouble is shooted.

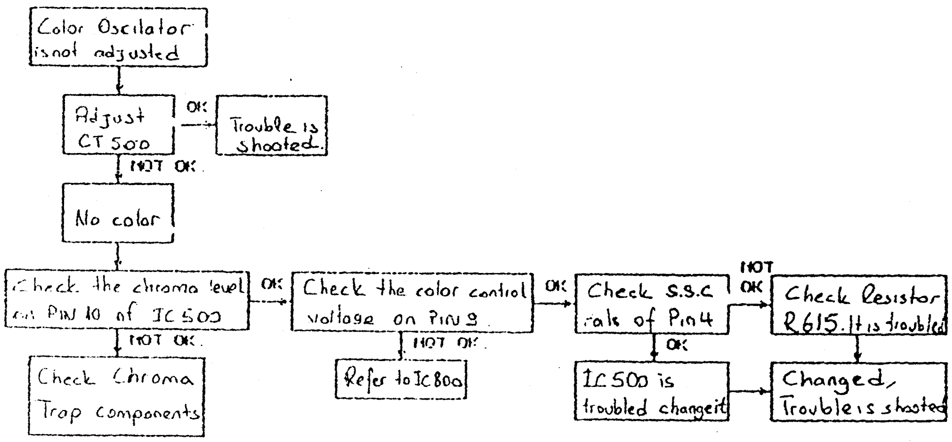
6) All the checkings were done but There's no O.S.D.


Check IC 800
22, 23, 24 and 25 Pins
OK
Socket CN502
is troubled.
NOT OK
IC 800 is
Troubled

7) White Screen, Fly Back Lines Present


Check 170V.
NOT OK
R 638
Open Circuit
Change resistor
Trouble is shooted.
OK
Check CRT Card's
T901, 902, 903
Transistor
NOT OK.
for 2 Transistors
are troubled Change
them
Trouble is shooted
OK
Picture Tube
is troubled
Changed and
trouble is shooted

8) No Color.


Color Oscilator
is not adjusted
Adjust
CT 500
OK
Trouble is
shooted.
NOT OK.
No color
Check the chroma level
on PIN 10 of IC 500
OK
Check the color control
voltage on Pin 9
OK
Check S.S.C
rals of Pin 4
NOT OK
Check Resistor
R615. It is troubled
NOT OK.
Check Chroma
Trap components
NOT OK.
Refer to IC 800
OK
IC 500 is
troubled changeit
Changed,
Trouble is shooted

9) No Color in Secam Moda

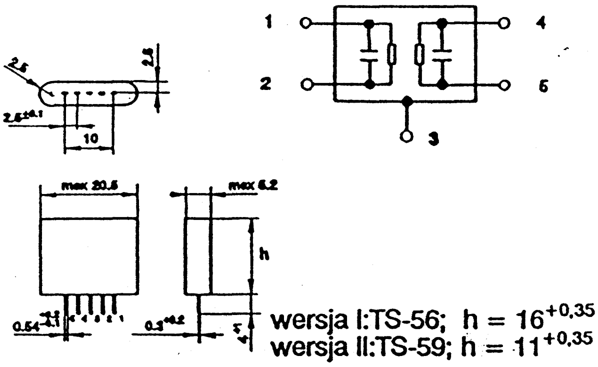
In General TDA3592A
is troubled Changeit

FILTR FT-389

ZASTOSOWANIA
Odbiorniki telewizyjne i magnetowidy (filtry do torów p.cz.)

STANDARD
D/K-OIRT, B/G-CCIR

OBUDOWA
Tworzywowa jednorzędowa typu TS-56 (wersja I) lub TS-59 (wersja II), hermetyczna



wersja I:TS-56; $h = 16^{+0,35}$
wersja II:TS-59; $h = 11^{+0,35}$

Układ wyprowadzeń
- 1 - wejście
- 2 - wejście łączone z masą układu
- 3 - masa układu
- 4,5 - wyjście (symetryczne)

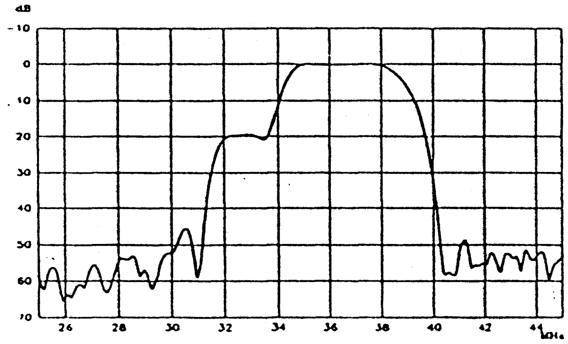
Parametr		Wartość	Jednostka
Tłumienność wtrąceniowa	37,40 MHz	max 20	dB
Poziom odniesienia dla podanych niżej wartości			
Tłumienność względna			
nośna wizji	38,90 MHz	4,2÷6,2	dB
podnośna chrominancji	34,47 MHz	-1,0÷4,6	dB
nośna fonii I	32,40 MHz	13÷22	dB
nośna fonii II	33,40 MHz	18÷22	dB
nośna wizji sąsiedniego kanału	30,90 MHz	min 45	dB
nośna fonii sąsiedniego kanału	40,40 MHz	min 44	dB
dolne pasmo zaporowe	25,00÷30,90 MHz	min 40	dB
górne pasmo zaporowe	40,40÷45,00 MHz	min 40	dB
Tłumienie sygnałów odbitych		min 44	dB
Tłumienie sygnału bezpośredniego przeniku elektromagnetycznego		min 50	dB
Opóźnienie grupowe			
częstotliwość odniesienia	38,90 MHz	0	ns
	36,20 MHz	typ -60	ns
podnośna chrominancji	34,47 MHz	typ -10	ns
Współczynnik temperaturowy		-72	ppm/K

PARAMETRY ELEKTRYCZNE

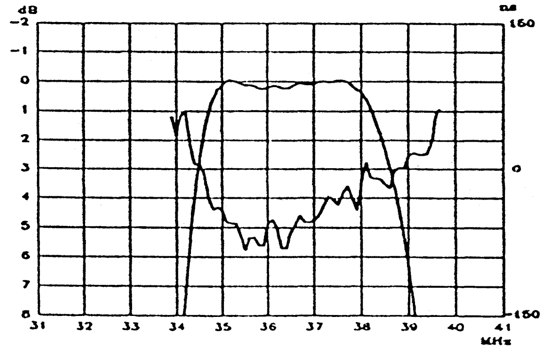
Dopuszczalne wartości napięć wejściowych
- napięcie stałe (krótkotrwałe): max 20 V
- amplituda sygnału w. cz.: max 10 V

Warunki pomiaru
- temperatura otoczenia: 23 °C
- impedancja sterująca: 50 Ω
- impedancja obciążenia: 2,0 kΩ ‖ 3pF

CHARAKTERYSTYKA AMPLITUDOWA



CHARAKTERYSTYKA AMPLITUDOWA I ZMIANY OPÓŹNIENIA GRUPOWEGO

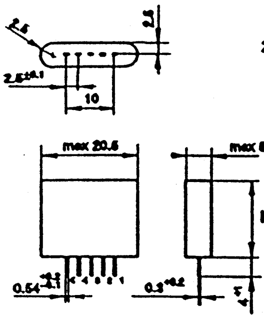


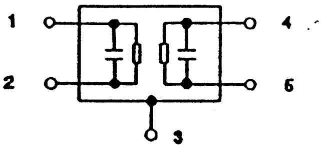
FILTR FT-3895

ZASTOSOWANIA
Odbiorniki telewizyjne i magnetowidy (filtry do torów p.cz.)

STANDARD
D/K-OIRT, B/G-CCIR

OBUDOWA
Tworzywowa jednorzędowa typu TS-56 (wersja I) lub TS-59 (wersja II), hermetyczna





wersja I:TS-56; $h = 16^{+0,35}$
wersja II:TS-59; $h = 11^{+0,35}$

Układ wyprowadzeń
1 - wejście
2 - wejście łączone z masą układu
3 - masa układu
4,5 - wyjście (symetryczne)

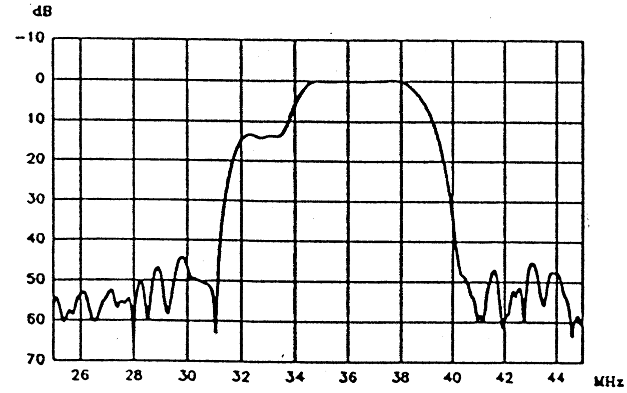
Parametr		Wartość	Jednostka
Tłumienność wtrąceniowa	37,40 MHz	max 18,5	dB
Poziom odniesienia dla podanych niżej wartości			
Tłumienność względna			
nośna wizji	38,90 MHz	4,4÷6,4	dB
podnośna chrominancji	34,47 MHz	0,3÷2,3	dB
nośna fonii I	32,40 MHz	12÷14,8	dB
nośna fonii II	33,40 MHz	12÷14,8	dB
nośna wizji sąsiedniego kanału	30,90 MHz	min 45	dB
nośna fonii sąsiedniego kanału	40,40 MHz	min 44	dB
dolne pasmo zaporowe	25,00÷30,90 MHz	min 40	dB
górne pasmo zaporowe	40,40÷45,00 MHz	min 40	dB
Tłumienie sygnałów odbitych		min 44	dB
Tłumienie sygnału bezpośredniego przeniku elektromagnetycznego		min 50	dB
Opóźnienie grupowe			
częstotliwość odniesienia	38,90 MHz	0	ns
	36,00 MHz	typ -90	ns
	36,70 MHz	typ -40	ns
podnośna chrominancji	34,47 MHz	typ 0	ns
Współczynnik temperaturowy		-72	ppm/K

PARAMETRY ELEKTRYCZNE

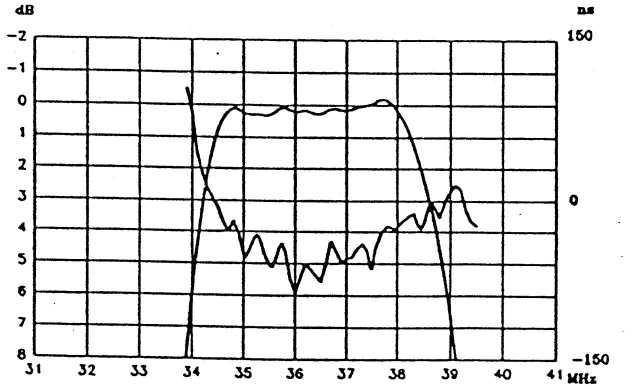
Dopuszczalne wartości napięć wejściowych
- napięcie stałe (krótkotrwałe): max 20 V
- amplituda sygnału w. cz.: max 10 V

Warunki pomiaru
- temperatura otoczenia: 23 °C
- impedancja sterująca: 50 Ω
- impedancja obciążenia: 2,0 kΩ ‖ 3pF

CHARAKTERYSTYKA AMPLITUDOWA



CHARAKTERYSTYKA AMPLITUDOWA I ZMIANY OPÓŹNIENIA GRUPOWEGO

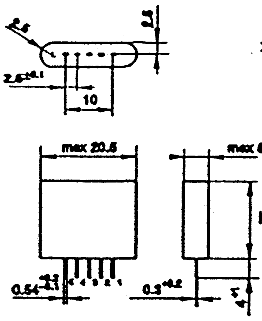


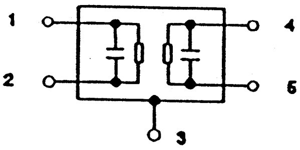
FILTR FT-3896

ZASTOSOWANIA
Odbiorniki telewizyjne i magnetowidy (filtry do torów p.cz.)

STANDARD
D/K-OIRT, B/G-CCIR

OBUDOWA
Tworzywowa jednorzędowa typu TS-56 (wersja I) lub TS-59 (wersja II), hermetyczna





wersja I:TS-56; $h = 16^{+0,35}$
wersja II:TS-59; $h = 11^{+0,35}$

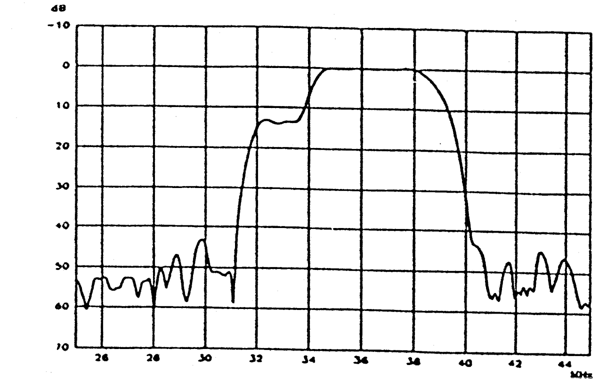
Układ wyprowadzeń
1 - wejście
2 - wejście łączone z masą układu
3 - masa układu
4,5 - wyjście (symetryczne)

PARAMETRY ELEKTRYCZNE

Dopuszczalne wartości napięć wejściowych
- napięcie stałe (krótkotrwałe): max 20 V
- amplituda sygnału w. cz.: max 10 V

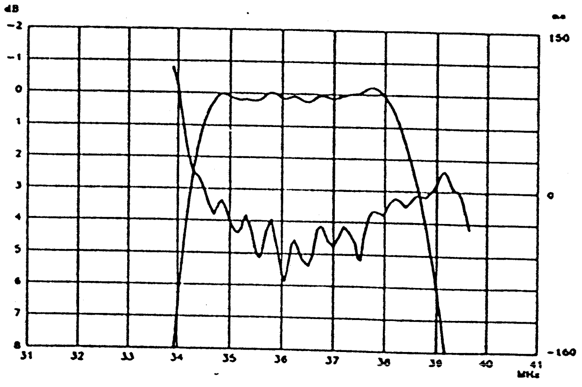
Warunki pomiaru
- temperatura otoczenia: 23 °C
- impedancja sterująca: 50 Ω
- impedancja obciążenia: 2,0 kΩ ‖ 3pF

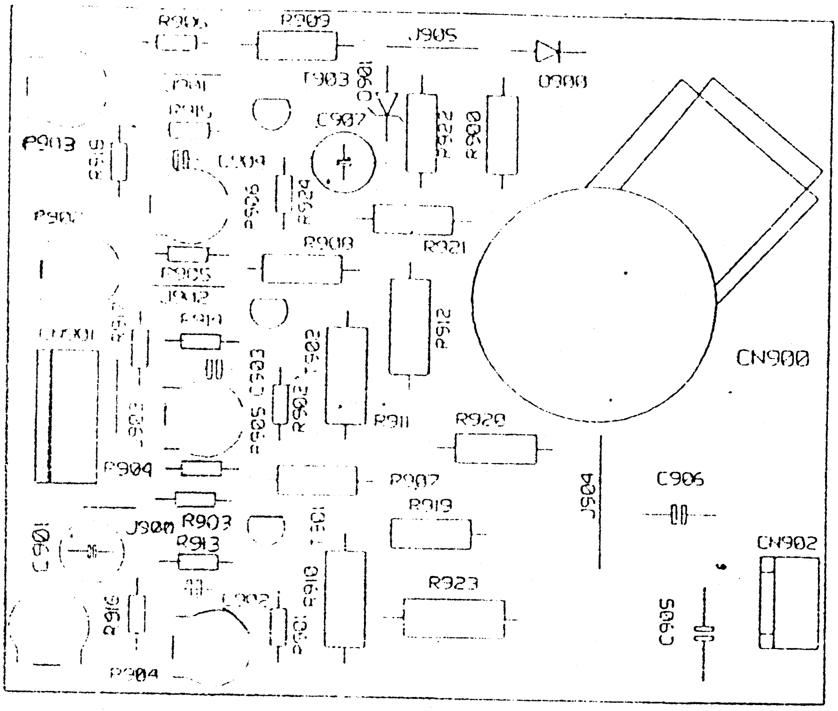
CHARAKTERYSTYKA AMPLITUDOWA



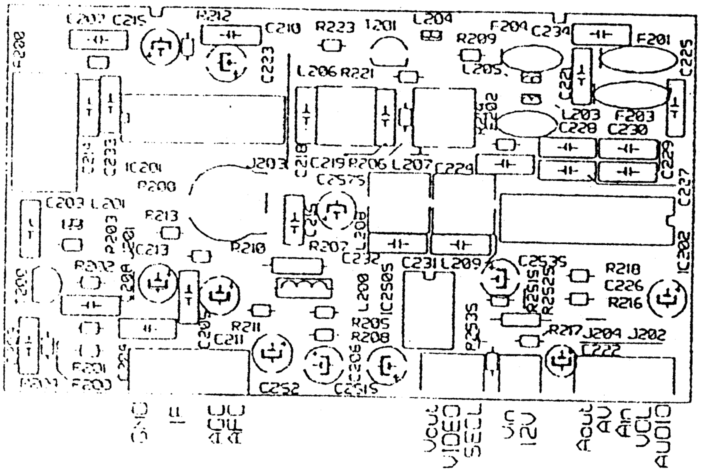
Parametr		Wartość	Jednostka
Tłumienność wtrąceniowa	37,40 MHz	max 18,5	dB
Poziom odniesienia dla podanych niżej wartości			
Tłumienność względna			
nośna wizji	38,90 MHz	4,4÷6,4	dB
podnośna chrominancji	34,47 MHz	0,3÷2,3	dB
nośna fonii I	32,40 MHz	12÷14,8	dB
nośna fonii II	33,40 MHz	12÷14,8	dB
nośna wizji sąsiedniego kanału	30,90 MHz	min 44	dB
nośna fonii sąsiedniego kanału	40,40 MHz	min 40	dB
dolne pasmo zaporowe	25,00÷30,90 MHz	min 40	dB
górne pasmo zaporowe	40,40÷45,00 MHz	min 36	dB
Tłumienie sygnałów odbitych		min 44	dB
Tłumienie sygnału bezpośredniego przeniku elektromagnetycznego		min 50	dB
Opóźnienie grupowe			
częstotliwość odniesienia	38,90 MHz	0	ns
	36,00 MHz	typ -75	ns
	-36,70 MHz	typ -40	ns
podnośna chrominancji	34,47 MHz	typ 0	ns
Współczynnik temperaturowy		-72	ppm/K

CHARAKTERYSTYKA AMPLITUDOWA I ZMIANY OPÓŹNIENIA GRUPOWEGO

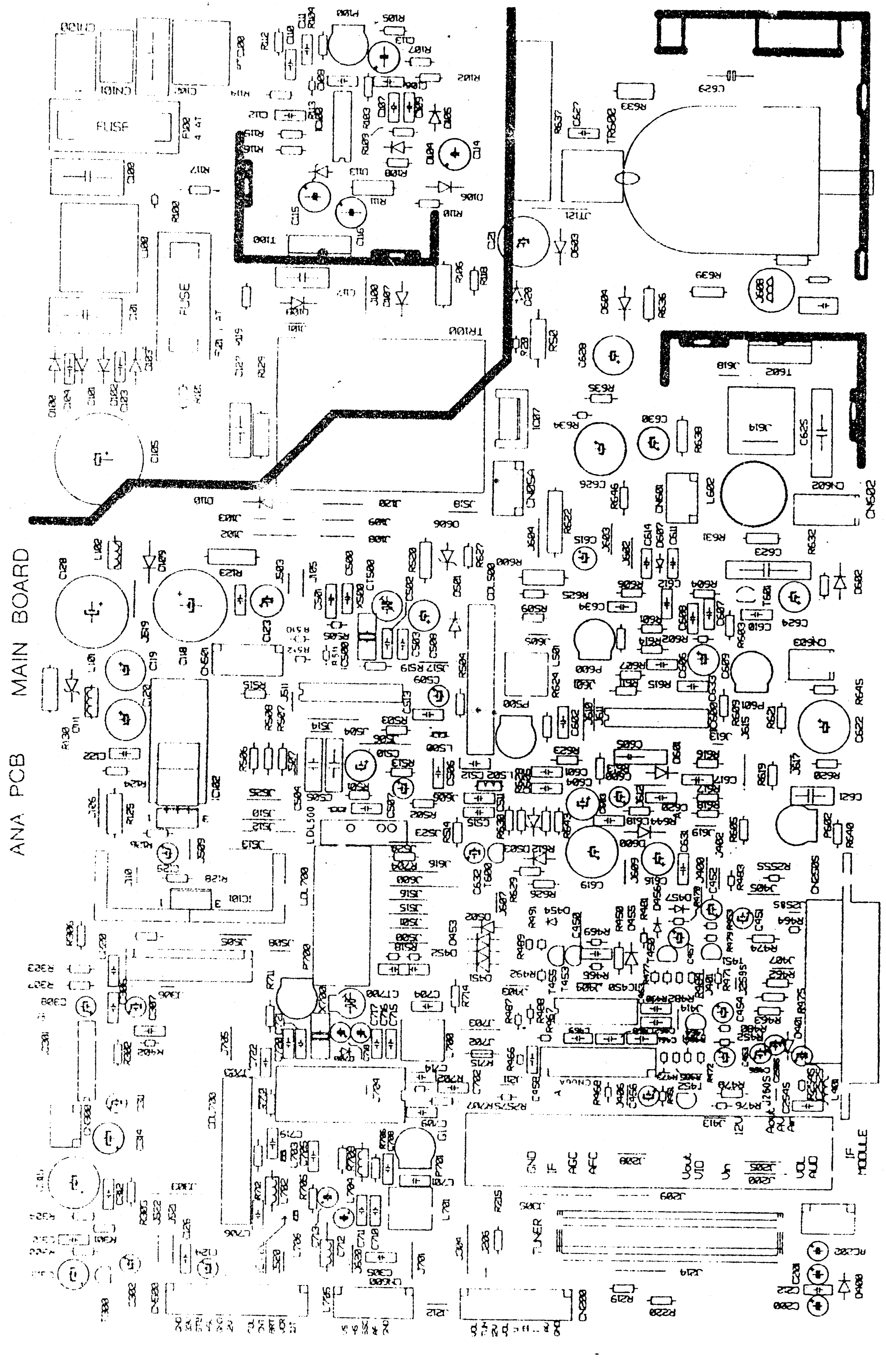



R906
R909
J905
D908
T903
D901
C907
R922
R900
R903
R915
C904
R906
R924
R902
R908
R921
R905
J912
R914
C900
R917
R912
CN900
C903
T902
R905
R902
R911
R920
R904
R907
J904
C906
R919
J900
R903
R913
T901
C901
CN902
R923
R916
C902
R910
R901
C905
R904

PL2 CRT BOARD


C207
C215
R212
C210
R223
T201
L204
F204
C234
F201
C225
R209
L205
C223
L206
R221
C221
R202
L203
F203
C228
C230
C229
C227
C214
C233
IC201
R200
J203
C218
C219
R206
L207
C224
C257S
C203
L201
R203
R213
C213
R210
R207
L208
C232
C231
L209
C253S
R218
C226
R216
IC202
R232
C209
C211
R211
R205
R208
IC250S
C206
R251S
R252S
R253S
R217
J204
J202
C222
C252
C251S
F201
F203
GND
IF
AGC
AFC
Vout
VIDEO
SECL
Vin
12V
Aout
AV
Ain
VCL
AUDIO

PL2 IF BOARD


ANA PCB MAIN BOARD
TUNER
IF MODULE
GND
IF
AGC
AFC
Vout
VIO
VOL
AUD
12V
FUSE
TR100
T100
T602
TR600
LDL700
LDL500
IC101
IC102
CN101
CN100
CN600
CN200
CN602
CN603
CN502

TDA1905

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, T_{amb} = 25°C, R_{th} (hea
20°C/W, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.
V_s	Supply voltage		4		30
V_o	Quiescent output voltage	V_s = 4V V_s = 14V V_s = 30V	1.6 6.7 14.4	2.1 7.2 15.5	2.5 7.8 16.8
I_d	Quiescent drain current	V_s = 4V V_s = 14V V_s = 30V		15 17 21	35
$V_{CE\ sat}$	Output stage saturation voltage	I_C = 1A I_C = 2A		0.5 1	
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 4Ω (•) V_s = 14V R_L = 4Ω V_s = 18V R_L = 8Ω V_s = 24V R_L = 16Ω	2.2 5 5 4.5	2.5 5.5 5.5 5.3	
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 14V R_L = 4Ω P_o = 50 mW to 3W V_s = 18V R_L = 8Ω P_o = 50 mW to 3W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		0.1 0.1 0.1 0.1	
V_i	Input sensitivity	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		37 49 73 100	
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4		
R_i	Input resistance (pin 8)	f = 1KHz	60	100	
I_d	Drain current	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		380 550 410 295	
η	Efficiency	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		73 71 74 75	

(•) With an external resistor of 100Ω between pin 3 and $+V_s$.

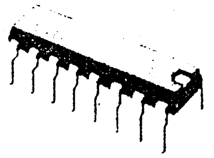
TDA1905

5W AUDIO AMPLIFIER WITH MUTING

The TDA1905 is a monolithic integrated circuit POWERDIP package, intended for use as low quency power amplifier in a wide range of pplications in radio and TV sets:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise
- voltage range 4V to 30V

The TDA 1905 is assembled in a new plastic ackage, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6W and a thermal resistance of 15°C/W (junction to pins).



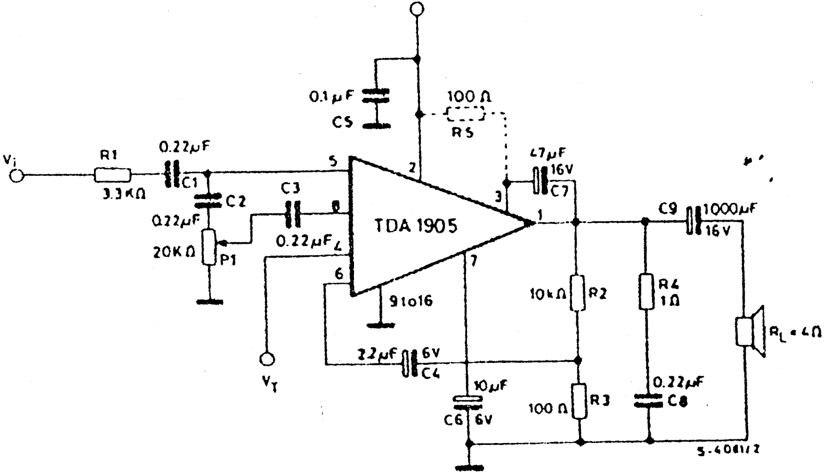
Powerdip
(8 + 8)

ORDERING NUMBER: TDA1905

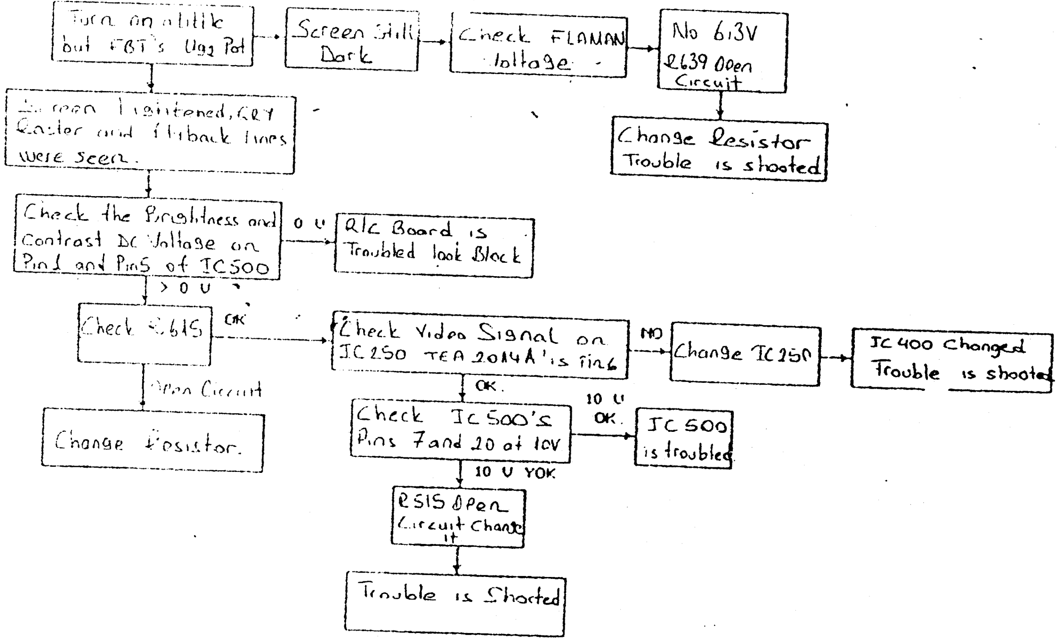
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3	A
I_o	Output peak current (repetitive)	2.5	A
V_i	Input voltage	0 to $-V_s$	V
V_i	Differential input voltage	±7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at $T_{amb} = 80°C$	1	W
	$T_{case} = 60°C$	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

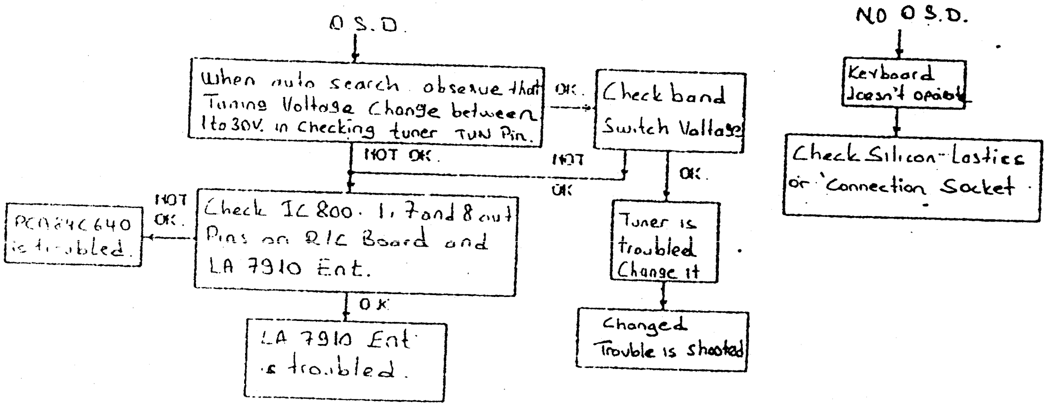
APPLICATION CIRCUIT


+Vs
0.1μF
C5
100 Ω
R5
Vi
R1
3.3KΩ
0.22μF
C1
C2
0.22μF
20KΩ
P1
C3
0.22μF
5
2
3
8
4
6
7
1
TDA 1905
9 to 16
VT
22μF
6V
C4
10μF
C6
6V
47μF
16V
C7
10kΩ
R2
100 Ω
R3
R4
1Ω
0.22μF
C8
C9
1000μF
16V
RL = 4Ω
S-4081/2

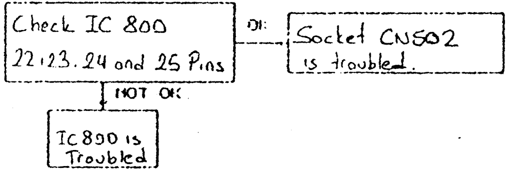
4> Dark Screen , Sound Present


Turn on a little but FBT's Ug2 Pot
Screen Still Dark
Check FLAMAN Voltage
No 6,3V R639 Open Circuit
Change Resistor Trouble is shooted
Screen lightened, GRY Raster and flyback lines were seen.
Check the Brightness and Contrast DC Voltage on Pin1 and Pin5 of IC500
0 V
R/C Board is Troubled look Block
> 0 V
Check R615
OK
Open Circuit
Change Resistor.
Check Video Signal on IC250 TEA 2014A's Pin6
NO
Change IC250
IC400 Changed Trouble is shooted
OK.
Check IC500's Pins 7and 20 at 10V
10 V OK.
IC500 is troubled
10 V YOK
R515 Open Circuit Change it
Trouble is Shooted

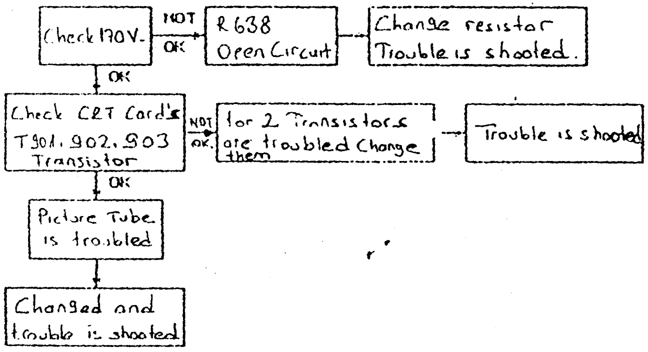
5> Snowly Screen , Station not found


O.S.D.
When auto search observe that Tuning Voltage Change between 1to30V. in Checking tuner TUN Pin.
OK.
Check band Switch Voltage
NOT OK.
NOT OK
OK.
Tuner is troubled Change it
Changed Trouble is shooted
NOT OK.
Check IC800. 1, 7and 8 out Pins on R/C Board and LA 7910 Ent.
PCA84C640 is troubled.
OK
LA 7910 Ent is troubled.
NO O.S.D.
Keyboard doesn't operate
Check Silicon-Lastics or Connection Socket

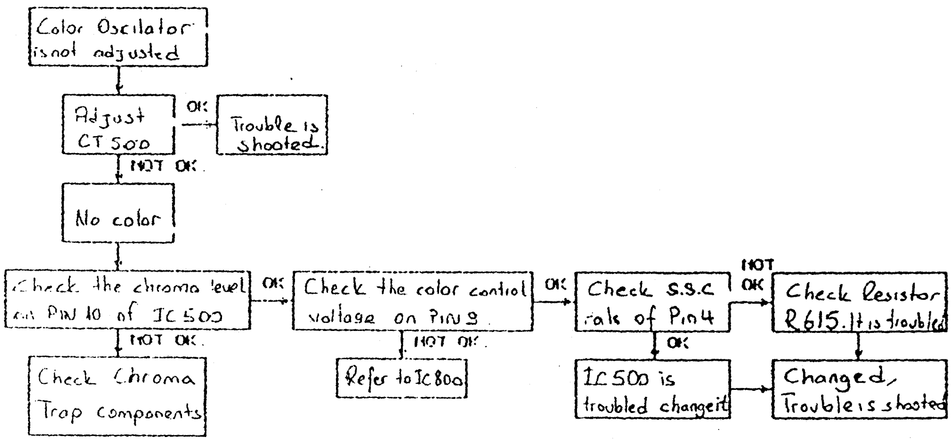
6) All the checkings were done but There's no O.S.D.


Check IC 800 22.23.24 and 25 Pins
OK
Socket CN502 is troubled.
NOT OK
IC 800 is Troubled

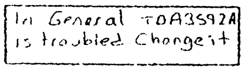
7) White Screen, Fly Back Lines Present


Check 170V.
NOT OK
R 638 Open Circuit
Change resistor Trouble is shooted.
OK
Check CRT Card's T901.902.903 Transistor
NOT OK.
for 2 Transistors are troubled Change them
Trouble is shooted
OK
Picture Tube is troubled
Changed and trouble is shooted

8) No Color.


Color Oscilator is not adjusted
Adjust CT 500
OK
Trouble is shooted.
NOT OK.
No color
Check the chroma level on PIN 10 of IC 500
OK
NOT OK.
Check Chroma Trap components
Check the color control voltage on Pin 9
OK
NOT OK.
Refer to IC 800
Check S.S.C vals of Pin 4
NOT OK
Check Resistor R615. It is troubled
OK
IC 500 is troubled changeit
Changed, Trouble is shooted

9) No Color in Secam Moda

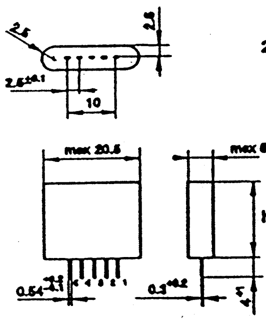

In General TDA3592A is troubled Change it

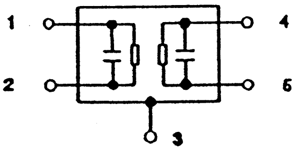
FILTR FT-389

ZASTOSOWANIA
Odbiorniki telewizyjne i magnetowidy (filtry do torów p.cz.)

STANDARD
D/K-OIRT, B/G-CCIR

OBUDOWA
Tworzywowa jednorzędowa typu TS-56 (wersja I) lub TS-59 (wersja II), hermetyczna





wersja I:TS-56; $h = 16^{+0,35}$
wersja II:TS-59; $h = 11^{+0,35}$

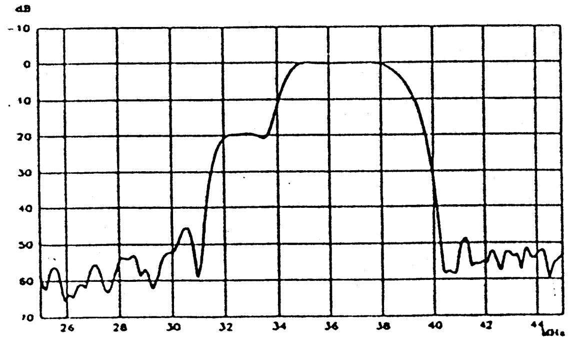
Układ wyprowadzeń
- 1 - wejście
- 2 - wejście łączone z masą układu
- 3 - masa układu
- 4,5 - wyjście (symetryczne)

PARAMETRY ELEKTRYCZNE
Dopuszczalne wartości napięć wejściowych
- napięcie stałe (krótkotrwałe): max 20 V
- amplituda sygnału w. cz.: max 10 V

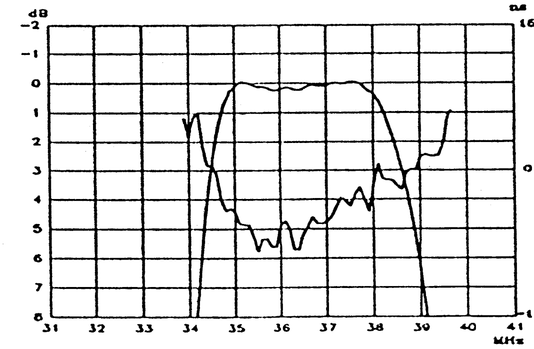
Warunki pomiaru
- temperatura otoczenia: 23 °C
- impedancja sterująca: 50 Ω
- impedancja obciążenia: 2,0 kΩ ‖ 3pF

Parametr		Wartość	Jednostka
Tłumienność wtrąceniowa	37,40 MHz	max 20	dB
Poziom odniesienia dla podanych niżej wartości			
Tłumienność względna			
nośna wizji	38,90 MHz	4,2÷6,2	dB
podnośna chrominancji	34,47 MHz	-1,0÷4,6	dB
nośna fonii I	32,40 MHz	13÷22	dB
nośna fonii II	33,40 MHz	18÷22	dB
nośna wizji sąsiedniego kanału	30,90 MHz	min 45	dB
nośna fonii sąsiedniego kanału	40,40 MHz	min 44	dB
dolne pasmo zaporowe	25,00÷30,90 MHz	min 40	dB
górne pasmo zaporowe	40,40÷45,00 MHz	min 40	dB
Tłumienie sygnałów odbitych		min 44	dB
Tłumienie sygnału bezpośredniego przeniku elektromagnetycznego		min 50	dB
Opóźnienie grupowe			
częstotliwość odniesienia	38,90 MHz	0	ns
	36,20 MHz	typ -60	ns
podnośna chrominancji	34,47 MHz	typ -10	ns
Współczynnik temperaturowy		-72	ppm/K

CHARAKTERYSTYKA AMPLITUDOWA



CHARAKTERYSTYKA AMPLITUDOWA I ZMIANY OPÓŹNIENIA GRUPOWEGO



FILTR FT-3895

ZASTOSOWANIA

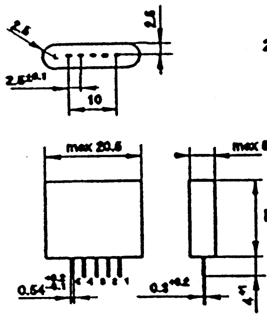
Odbiorniki telewizyjne i magnetowidy (filtry do torów p.cz.)

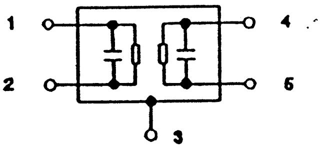
STANDARD

D/K-OIRT, B/G-CCIR

OBUDOWA

Tworzywowa jednorzędowa typu TS-56 (wersja I) lub TS-59 (wersja II), hermetyczna





wersja I:TS-56; $h = 16^{+0,35}$
wersja II:TS-59; $h = 11^{+0,35}$

Układ wyprowadzeń
1 - wejście
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4,5 - wyjście (symetryczne)

PARAMETRY ELEKTRYCZNE

Dopuszczalne wartości napięć wejściowych

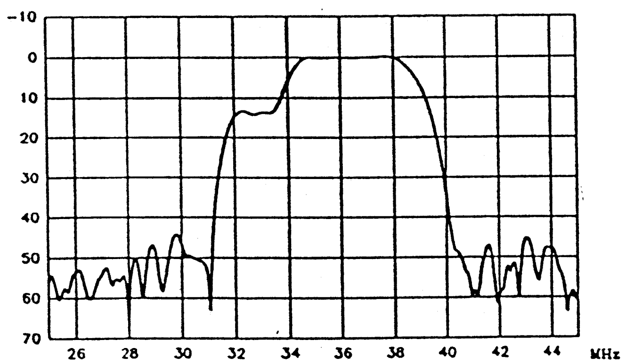
- napięcie stałe (krótkotrwałe): max 20 V
- amplituda sygnału w. cz.: max 10 V

Warunki pomiaru

- temperatura otoczenia: 23 °C
- impedancja sterująca: 50 Ω
- impedancja obciążenia: 2,0 kΩ || 3pF

Parametr		Wartość	Jednostka
Tłumienność wtrąceniowa	37,40 MHz	max 18,5	dB
Poziom odniesienia dla podanych niżej wartości			
Tłumienność względna			
nośna wizji	38,90 MHz	4,4÷6,4	dB
podnośna chrominancji	34,47 MHz	0,3÷2,3	dB
nośna fonii I	32,40 MHz	12÷14,8	dB
nośna fonii II	33,40 MHz	12÷14,8	dB
nośna wizji sąsiedniego kanału	30,90 MHz	min 45	dB
nośna fonii sąsiedniego kanału	40,40 MHz	min 44	dB
dolne pasmo zaporowe	25,00÷30,90 MHz	min 40	dB
górne pasmo zaporowe	40,40÷45,00 MHz	min 40	dB
Tłumienie sygnałów odbitych		min 44	dB
Tłumienie sygnału bezpośredniego przeniku elektromagnetycznego		min 50	dB
Opóźnienie grupowe			
częstotliwość odniesienia	38,90 MHz	0	ns
	36,00 MHz	typ -90	ns
	36,70 MHz	typ -40	ns
podnośna chrominancji	34,47 MHz	typ 0	ns
Współczynnik temperaturowy		-72	ppm/K

CHARAKTERYSTYKA AMPLITUDOWA



CHARAKTERYSTYKA AMPLITUDOWA I ZMIANY OPÓŹNIENIA GRUPOWEGO